2nd India ESD Workshop: The Heart of Innovation

Venue: Faculty Hall, Main Building, IISc Bangalore

Date: 17th March 2017

Hosted by: MSDLab @ Indian Institute of Science Bangalore

With desideratum of conducting ESD workshop last year and getting positive feedback resulted in its conduct once again. MSDLab @ IISc Bangalore (India) and ESD Association (USA) envisioned this workshop so as to heighten and develop ESD design activities in India through this forum known as "India ESD Forum". IEW highlights four-fold vision. First, to increase ESD awareness among engineers and academicians working in the field of VLSI Microelectronics and would like to learn or engage into ESD protection device/circuit/product design and testing activities. Second, to bring engineers together who encounter ESD problems in their designs. Third, to promote research, development and training related to on-chip ESD device/circuit design in India. Finally, the most prominent, to use this model to strengthen Academia-Industry partnership in and around country.

Prof. Mayank Shrivastava, IISc, commenced the workshop by giving a brief overview. Great interest being shown by VLSI professionals, industry professionals from semiconductor giants made this event a milestone. Compared to last year, more than 60 industry professionals from multinational corporations like SanDisk, Intel, NXP, Cadence, Infineon, and Synopsys engaged (Fig. 1). Also, intense student volunteer (about 20) and faculty member participation led to a smooth planning and administration of the workshop (Fig. 2). Riveting and thorough technical discussions and sessions pertaining to latest System Level/ IC Level ESD design issues were conducted. Unlike the previous IEW event, brainstorming sessions and contributed talks from the industry and student participants, prompted additional interest among the audience, and became the highlight of the 2nd IEW workshop.

ESD experts Dr. Harald Gossner, and Dr. Wolfgang Stadler complemented the "Ask the Experts" session through teleconferencing. This led to an elaborated and enlightening talk by Intel ESD expert, Dr. Harald Gossner, on SEED: System Efficient ESD Design. The event concluded with poster session, and feedbacks/suggestions for the future workshops (Fig. 3).

On the whole, it was a grand full- day event. The statistics clearly project its widespread recognition in the prevailing ESD society (Fig. 1). Looking at the inflating Academia-Industry participation compared to last year (2x hike), exponential growth of the IEW Forum can be undoubtedly forecasted. Aligning with the roadmap/feedbacks, the next workshop will be planned to have live Q/A sessions with the experts, engaging tutorials and focused topics/presentations outlined for a condensed event.

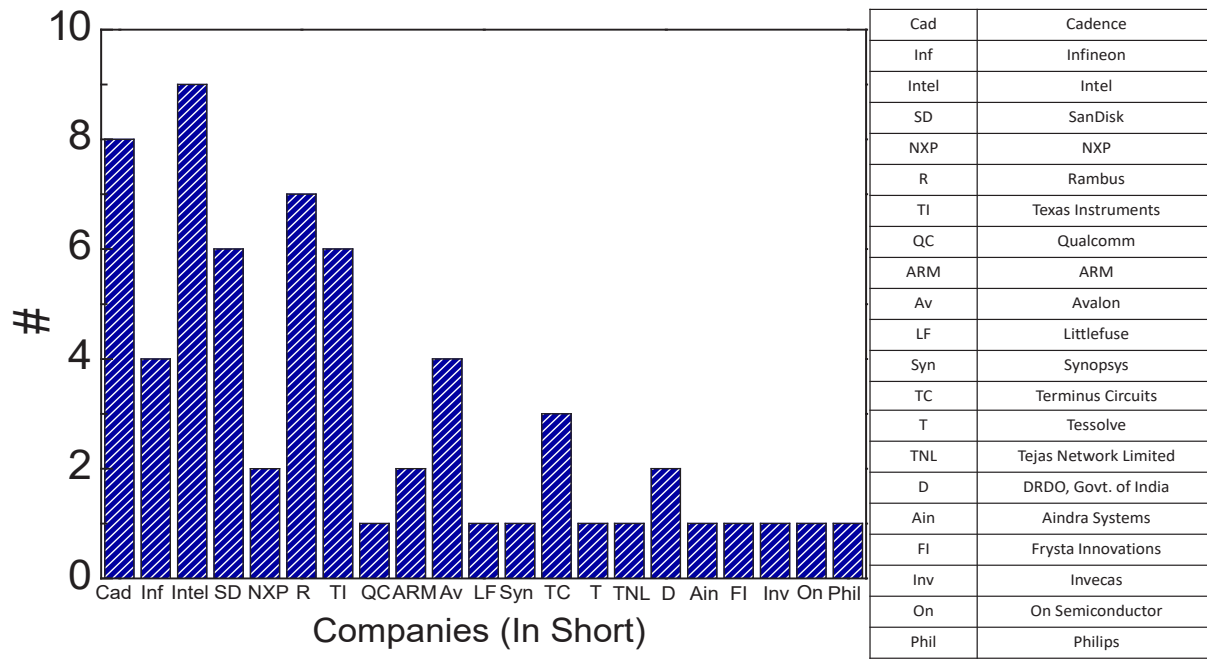|	
Cad	Cadence
Inf	Infineon
Intel	Intel
SD	SanDisk
NXP	NXP
R	Rambus
TI	Texas Instruments
QC	Qualcomm
ARM	ARM
Av	Avalon
LF	Littlefuse
Syn	Synopsys
TC	Terminus Circuits
T	Tessolve
TNL	Tejas Network Limited
D	DRDO, Govt. of India
Ain	Aindra Systems
FI	Frysta Innovations
Inv	Invecas
On	On Semiconductor
Phil	Philips

Fig. 1: Company wise distribution of participants.
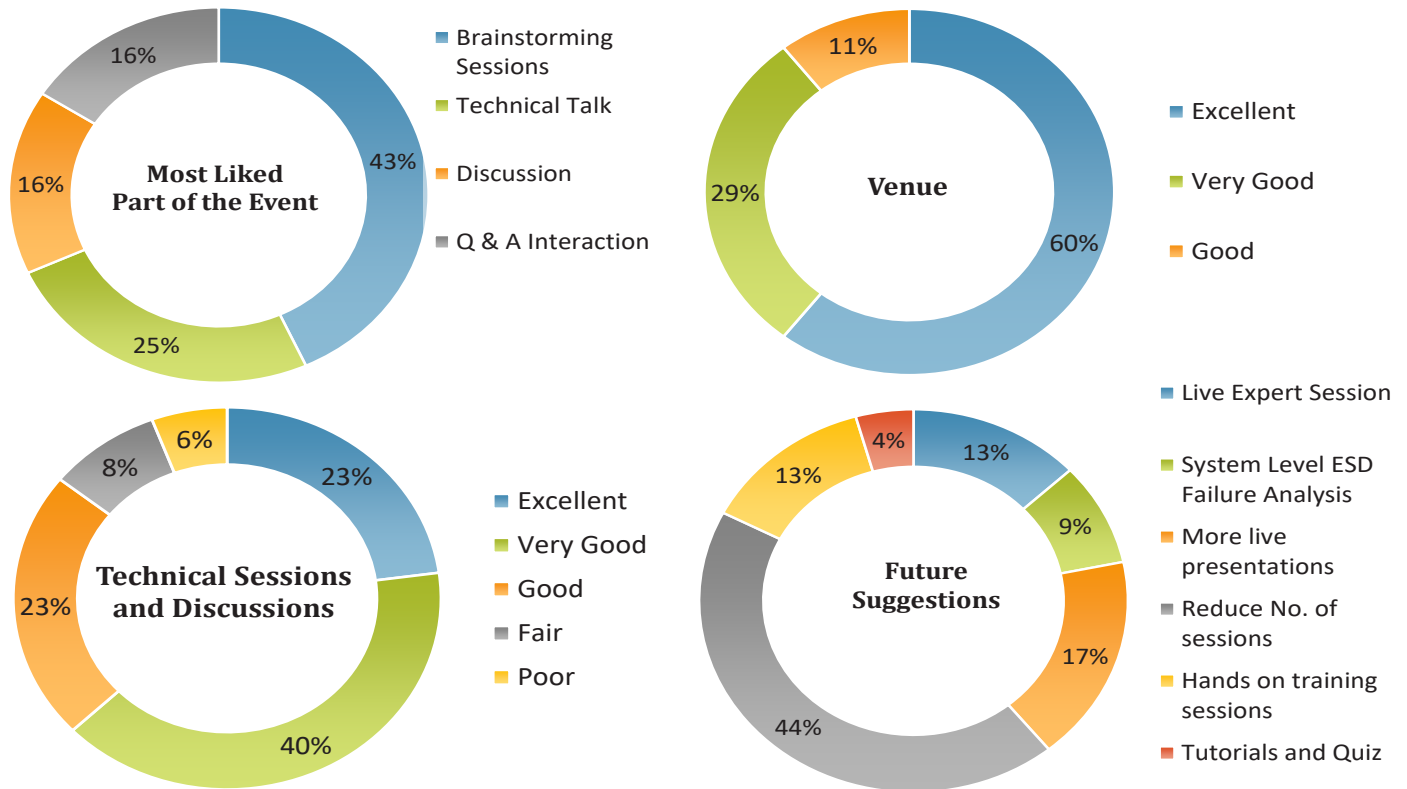

Fig. 2: Visuals from the workshop.

Fig. 3: Feedbacks and Suggestions.

About (upcoming) 3rd India ESD Workshop: With the last few years of successful InEW programs, this year (Feb 25th 2019) the highlight of the program will be (i) keynote and invited talks by the ESD experts of leading chip manufacturing companies around the world, (ii) DL talks by IEEE EDS DL having expertise in ESD, (iii) talks by lead engineers from leading chip design groups in Bangalore and (iv) poster presentation by various design engineers with a focus on their respective ESD needs. Besides, we will have an interactive session on Feb 26th between ESD experts and design engineers. Details of previous year event can be found here. This year we already have over 150 registrations with 90% industry presence. We are expecting to have around 250 participants eventually. Some of the key note speakers are experts like Dr. Harald Gossner (Intel), Prof. Mayank Shrivastava (IISc), Dr. Charvaka Duvvury (IEEE Fellow) and Dr. Gianluca Boselli (TI).