InEW 2024
India ESD Workshop

IEEE
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22nd - 23rd August 2024

5th India ESD Workshop

Indian Institute of Science, Bangalore, India

TECHNICAL PROGRAM

Venue: Indian Institute of Science, Bangalore
Organised By: Prof. Mayank Shrivastava (IISc)

Web: https://iisc-inew.org/
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InEW 2024 India ESD Workshop

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About the India ESD Workshop (InEW)

ESD reliability understanding and how to design ESD safe chips have always been highly important and crucial aspects for semiconductor design, development, testing, and manufacturing cycles. Given the absence of ESD design/testing/technology knowledge, expertise, and awareness in India, in 2015 **Indian Institute of Science (IISc), Bangalore** started efforts for industry professionals and students, which today is called **India ESD Workshop (InEW).** This conference has gathered significant interest and traction from the semiconductor industry professionals in India, with the potential to expand to other regions going forward. For example, the last edition attracted 250+ senior-level engineers from the semiconductor industry. The conference has also flourished due to its significant collaborations with industry leaders like Intel, Samsung, Texas Instruments, Western Digital, Global Foundry, Qualcomm, Synopsys, Cadence and NXP etc. The objective of the conference has always been to promote the knowledge, know-how, and expertise in ESD design, technology, and testing, in collaboration with global ESD experts. With the growing manufacturing requirements, manufacturing push in the country, upcoming fabs, an increasing number of chip design centers getting into full product cycles (full product developments), and an increasing number of chip design start-ups with efforts on end products, this expertise becomes more than relevant and justifies the need and growth of venues like InEW to continue and grow. With the current context, it would not be an exaggeration if the conference grows to 500+ professionals in the years to come.

Poster Session

An interactive Poster Session of 20 plus posters with High Tea. Participants get to see a variety of world class research done in the area of Electrostatic discharge and get to ask questions and engage in dialogue with the presenters.

Meet World Renowned Experts

A platform for poised to revolutionize the way industry leaders connect with top-tier talent. Our platform ensures that every expert in the field of Electrostatic Discharge is showcased to potential collaborators and employers on a global scale.

Industry Sessions

Heated and seated discussion sessions, in a relaxed setting, on emerging technological areas or key showstoppers or major scientific debates with a quest to find the role academia must play in the next 10 years.

Panel Discussion

To brainstorm on the major ESD induced bottlenecks in the cutting edge technologies and products in the Semiconductor Industry.

Industry Interaction

Conducting collaborative brainstorming sessions to explore opportunities for closer engagement with the industry. This initiative aims to establish a distinctive platform for fostering robust academia-industry partnerships, culminating in the development of a comprehensive 10-year plan and roadmap.

Young Researchers Meet

A special session to explore research opportunities in leading R&D Labs and academic institutions in India.

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Workshop Highlights

04 Keynote Talks	01 Panel Session
25 Technical Talks	10 Platform Presentations
25 Poster Presentations	300+ Attendees

Why Attend and Participate?

- Global Engagement: Collaborate with international ESD design experts, resolving design complexities and pioneering resilient ESD design and protection strategies.
- Cutting-edge Discoveries: Dive deep into innovative process technologies, gaining insights into their global implications and applications.
- Expansive Networking: Connect with global peers, industry leaders, and academics, establishing valuable partnerships for the future.
- Present and Propel: Showcase your work on a global stage, attracting diverse perspectives, accolades, and potentially setting industry standards.
- For Students: A unique platform to learn, shine, and perhaps, chart a future course with potential employers from across the globe.
- Relevance to the Global Community: At a time when electronic intricacies intersect with the demand for robustness and reliability, understanding ESD challenges is not just essential; it's critical. InEW-2024 promises to be the crucible where knowledge meets application, innovation meets industry, and challenges meet solutions. It aims to not only address current ESD challenges but also proactively envision and counter future hurdles, ensuring the global VLSI community stays ahead of the curve.

As we stand on the cusp of technological revolutions, with semiconductor technologies reaching their fundamental limits, and devices becoming smarter and more interconnected, the significance of ESD reliability cannot be overstated. Join us at India ESD Workshop 2024. Be part of this global movement, shaping the trajectory of On-Chip and System level ESD design and reliability physics in the realm of a plethora of semiconductor technologies. Together, let's drive a global ESD knowledge renaissance for a technologically resilient future.

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Topics of Interest

1. Advanced CMOS: FinFET, Nanowires, Nanosheets, etc.

ESD Issues in Advanced Technologies (Multi-gate, FinFET, SOI, SiGe, nanowire, etc.), On-Chip ESD Protection Devices & Techniques in Advanced CMOS Technologies, IC Design and Layout Issues, Circuit Simulation of EOS/ESD Events in Advanced CMOS Technologies, DC/Transient Latch-up Issues and Solutions.

2. Emerging Technologies: 2D, RRAM, Neuromorphic Devices, Quantum, etc.

ESD issues in novel devices with 2D layered semiconductor or dielectric materials, logic and memory devices, neuromorphic devices, quantum devices and quantum enhanced technologies.

3. 2.5D & 3D Stacking, TSV, Backside Power Delivery Network

ESD Issues and solutions in 2.5D & 3D IC packaging and integration, interconnects, TSV, ESD protection requirements in Backside Power Delivery Network.

4. Analog & Automotive Technologies: Bipolar, RF, High Voltage, and BCD

ESD Issues, on-chip ESD protection devices and techniques, IC Design and layout issues, ESD circuit simulation and co-design, DC/Transient Latch-up Issues and Solutions in Bipolar, RF, High Voltage, and BCD Technologies.

5. ESD Testing

ESD Testing trends with Technology Scaling, Multi-dimensional packaging, ESD Test and Characterization method, Traditional and Novel TLP Testing System, HBM and CDM testing issues and solutions, Reliability Test equipment,New failure mechanism, Advance failure analysis techniques, ESD Checking and verification Technology.

6. ESD Device & System Modelling

System level Test, modeling and simulation method, Circuit level design and simulation of ESD Events in Advanced CMOS Technologies, Use of EDA tools, IC Design and Layout issues, Transient ESD induced upset, Robustness evaluation for standard test boards,Large scale analysis with machine and deep learning.

7. Numerical Modeling and Simulation of ESD Components

Component level ESD design including but not limited to SCR, LDMOS, GGNMOS, GDPMOS, Diode, etc., TCAD/Circuit Simulation, Numerical modeling and Physics od ESD events, Advance simulation technologies (SOI, SiGe, FinFET, Compound, Nanowire),Latchup detection prevention and mitigation, Simulation tools and methodology.

8. ESD CAD & Verification

ESD modeling, design guidelines, testing standards, whole chip ESD protection, design verification, compliance testing, ESD Protection for mixed voltage applications.

9. System Level ESD

System efficient ESD design (SEED), ESD testing standards (IEC), co-design methodology of on-board and on-chip ESD protection, ESD protection for consumer electronics, automotive, aerospace and industrial applications, Advancements in System level IEC qualification test methods like Air-discharge tests, Development challenges related to off-chip protection elements with ultra-low capacitances.

10. ESD and EOS Protection in GaN HEMTs & GaN Power ICs

GaN technology based ESD protection diodes, TVS, testing and shielding techniques, EOS protection from overvoltage conditions, current surges and power supply instability.

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Key Dates

May 10th	Poster Submission
June 15th	Poster Acceptance
June 30th	Program Announcement
July 31st	Early Bird Registration Deadline
August 21st	Late Registration Deadline
August 22nd-23rd	India ESD Workshop

InEW 2024 India ESD Workshop

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Program Schedule

Day 1 (22th Thursday August)

Time	Duration	Speaker & Affiliation	Talk Details
08:30 AM	45 Mins	**Registration and Networking**	
09:15 AM	15 Mins	**Welcome and Inauguration**	
09:30 AM	45 Mins	**Dr. Harald Gossner** (Intel, Germany)	The Picosecond Challenge in CDM Testing – endangering ESD Robustness of Highspeed Interfaces (Keynote)
10:15 AM	45 Mins	**Prof. Elyse Rosenbaum** (UIUC, USA)	ESD Design for High-speed Wireline IOs in Advanced CMOS Technologies (Keynote)
11:00 AM	30 Mins	**Break**	**Break**
11:30 AM	30 Mins	**Mr. Mototsugu Okushima** (Renesas Electronics, Japan)	Efficient CDM Protection Design for Cross Power Domain of Analog/RF block in Finfet Technology (Invited)
12:00 PM	30 Mins	**Dr. Teruo Suzuki** (Socionext Inc., Japan)	Consideration based on ESD applied waveform in High-Speed IF using T-Coil (Invited)
12:30 PM	30 Mins	**Dr. Dolphin Abessolo Bidzo** (NXP Semiconductors, The Netherlands)	Electronic Design Automation (EDA) Layout Verification Methodology for Charged Device Model (CDM) (Invited)
01:00 PM	90 Mins	**Networking Lunch**	**Networking Lunch**
02:30 PM	30 Mins	**Dr. Hossam Sarhan** (Siemens, USA)	Ensuring Sign-off Design Reliability: Navigating Complex Requirements using Calibre® PERC™
03:00 PM	30 Mins	**Mitesh Goyal** (Indian Institute of Science)	Load-line Dependent Current Filament Dynamics in Nanoscale SCR Devices (PhD Talk)
03:30 PM	30 Mins	**Mohammad Ateeb Munshi** (Indian Institute of Science)	Understanding Temperature Dependence of ESD Reliability in AlGaN/GaN HEMTs (PhD Talk)
04:00 PM	30 Mins	**Rasik Rashid Malik** (Indian Institute of Science)	Interplay of Surface Passivation and Electric Field Distribution in Determining ESD Behaviour of p-GaN Gated AlGaN/GaN HEMTs (PhD Talk)
04:30 PM	30 Mins	**Coffee Break**	**Coffee Break**
05:00 PM	60 Mins	Moderator: **Prof. Mayank Shrivastava** (Indian Institute of Science)	Panel Session: Semiconductor Advancements & Growing ESD Challenges
06:00 PM	90 Mins	**Poster Session**	
07:30 PM	120 Mins	**Chair's Reception & Dinner**	

InEW 2024 India ESD Workshop

Program Schedule

Day 2 (23rd Friday August)

Time	Duration	Speaker & Affiliation	Talk Details
09:00 AM	45 Mins	**Dr. Gianluca Boselli** (Texas Instruments, USA)	System-Level ESD design challenges in HV Automotive Applications: process, IP and system co-design perspective (Keynote)
09:45 AM	45 Mins	**Dr. Charvaka Duvvury** (iT2 Technologies, USA)	Exploring Machine Learning for ESD Data Analysis (Keynote)
10:30 AM	20 Mins	**Prof. Mayank Shrivastava** (Indian Institute of Science)	Predictive TCAD-Based ESD Design without Foundry Data
10:50 AM	10 Mins	**Mr. Sharath B N** (COMSOL)	Multiphysics Simulation for the Semiconductor Industry
11:00 AM	30 Mins	**Break**	**Break**
11:30 AM	30 Mins	**Dr. Matteo Buffolo** (University of Padova, Italy)	Robustness of GaN-based LED against EOS events and ESDs (Invited)
12:00 PM	30 Mins	**Ms. Yang Yanjing** (ThermoFisher Scientific, Singapore)	Failure Analysis workflow for Advanced Packing and Power Semiconductor Device (Invited)
12:30 PM	30 Mins	**Mr. Christopher Almeras** (Raytheon, USA)	Risk Mitigation in Manufacturing of High Reliability Product (Invited)
01:00 PM	90 Mins	**Networking Lunch**	**Networking Lunch**
02:30 PM	30 Mins	**Prof. David Pommerenke** (Technical University Graz, Austria)	System Efficient ESD Design
03:00 PM	30 Mins	**Dr. Kranthi Nagothu** (Texas Instruments, USA/India)	On-chip protection Design Challenges for system level ESD (Invited)
03:30 PM	30 Mins	**Monishmurali M** (Texas Instruments)	Addressing design challenges for current uniformity in Fin-based SCRs (PhD Talk)
04:00 PM	30 Mins	**Dr. Charvaka Duvvury** (iT2 Technologies, USA)	Green ESD: Efficient Test Methods to Save Time and Effort During Qualification

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Program Schedule

Day 2 (23rd Friday August)

04:30 PM	**30 Mins**	**Coffee Break**	**Coffee Break**
05:00 PM	**15 Mins**	**Anamika Chowdhury** (Lam Research)	Low Pressure Reactor Design to Avoid Unwanted Electrostatic Discharge
05:15 PM	**15 Mins**	**Anurag Mittal** (Synopsys, India)	I/O ESD implementation for 2.5D/3D Applications (Contributed)
05:30 PM	**15 Mins**	**Chinmayee Panigarhi** (NXP Semiconductors)	Challenges in ESD protection for High-Speed CML transmitter having thin oxide devices and their solution (Contributed)
05:45 PM	**15 Mins**	**Dattatreya Prabhu Rachakonda** (GlobalFoundries, India)	Learnings from Switch Self-Protection: From models to hardware (Contributed)
06:00 PM	**15 Mins**	**Harshit Dhakad** (Intel Technologies India Pvt.)	Tracing and debugging of ESD failures in a module assembly line (Contributed)
06:15 PM	**15 Mins**	**Gopikrishna Siddula** (Western Digital, India)	Enhancing Reliability in High speed and High-Density Storage: Practical Strategies for Mitigating Electrostatic Discharge (ESD) (Contributed)
06:30 PM	**15 Mins**	**Manohar Seetharam** (Samsung, India)	ESD design challenges and solutions for Mphy G5 transceiver design in 2/3nm (Contributed)
06:45 PM	**30 Mins**	**Networking, Poster and Hi-tea**	
07:15 PM	**15 Mins**	**Concluding remarks, Vote of thanks & 6th InEW Announcement**	

Panel Discussion

Panel Discussion: Semiconductor Advancements & Growing ESD Challenges
Date & Time: August 22, 2024, 5:00 PM - 6:00 PM
Moderator: Prof. Mayank Shrivastava, Indian Institute of Science

Session Overview

The semiconductor industry is undergoing rapid advancements, with new technologies pushing the boundaries of what is possible. However, these advancements also bring about new challenges, particularly in the realm of Electrostatic Discharge (ESD) protection. As semiconductor devices become smaller, faster, and more integrated, the need for robust ESD solutions becomes more critical. This panel session will bring together leading experts from academia and industry to discuss and debate the emerging ESD challenges associated with next-generation semiconductor technologies.

Panellists & Topics

Dr. Harald Gossner (Senior Principal Engineer, Intel Corporation, Germany)

Topic: Discussion on the evolution of CMOS nodes over the next 15 years, focusing on advanced and 3D packaging, heterogeneous integration, backside power rails, and the impact of newer materials like 2D materials on ESD design and protection.

Dr. Mototsugu Okushima (Senior Director, Renesas Electronics, Japan)

Topic: Exploration of ESD challenges in advanced automotive nodes, system-level ESD issues in electric vehicles (EVs), and the specific requirements of advanced automotive and EV applications.

Dr. Hossam Sarhan (Principal Engineer, Siemens EDA, USA)

Topic: Examination of the growing complexity of ESD issues and the role of advanced computational and simulation techniques in addressing these challenges. Emphasis on the need for more sophisticated simulation approaches as semiconductor technologies continue to evolve.

Prof. Elyse Rosenbaum (Professor, University of Illinois Urbana-Champaign, USA)

Topic: Insight into the unique ESD challenges posed by next generation and futuristic technologies. Discussion on the critical role that academia plays in addressing scientifically challenging problems that are beyond the current capabilities of industry, and the importance of industry-academia collaborations.

Session Format

- **Opening Statements (30 minutes):** Each panellist will present their thoughts on the designated topics, providing insights into the current state of ESD challenges and future directions. (7 minutes per panellist with a 30-second buffer for transitions).
- **Panel Debate & Discussion (10 minutes):** Panellists will engage in a debate, discussing and potentially challenging or supporting each other's views on the topics presented.
- **Audience Q&A (20 minutes):** The session will conclude with an interactive Q&A segment, allowing the audience to pose questions to the panellists and participate in the discussion.

Expected Outcomes

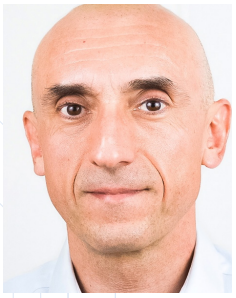
- Provide a comprehensive overview of the current and future ESD challenges in advanced semiconductor technologies.
- Facilitate a deep discussion on the role of emerging technologies in shaping ESD protection strategies. Encourage collaboration between industry and academia to address these challenges effectively.

Keynote & Invited Speakers

Dr. Harald Josef Erhard Gossner
Intel Deutschland GmbH

Talk Title: The Picosecond Challenge in CDM Testing–endangering ESD Robustness of Highspeed Interfaces

Abstract: Ultrafast transients during a Charged Device Model (CDM) ESD test have led to puzzling fails of high speed interfaces. It has been found that package and IC design solutions for high speed interfaces with a Nyquist frequency far above 5 Ghz become more and more transparent for CDM pulse slopes below 100 ps. While this was not considered as relevant in previous designs the combination of ultra-fast pulse transients, high bandwidth of the transmission channel to the gate oxide and the high overvoltage sensitivity of gate oxides in sub 3nm CMOS nodes causes a drop in ESD robustness far below a 250 V CDM target. The talk will present the effect and the modelling approach to correctly capture this effect during the ESD protection design phase.

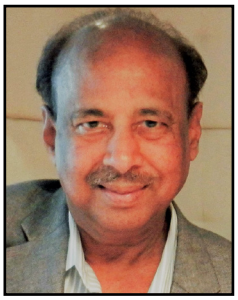


Dr. Gianluca Boselli
Texas Instruments

Talk Title: System-Level ESD design challenges in HV Automotive Applications: process, IP and system co-design perspective

Abstract: The trend towards society's "smart-electrification" is driving the need for ESD immunity at system-level. IEC 61000-4-2 defines how to perform the Electrostatic discharge immunity test at system level. To protect against these events, until fifteen years ago, ad-hoc ESD protections (TVS – Transient Voltage Suppressors) were implemented at board/ system - level in proximity of the connectors interfacing with the "external world". However, a new trend of implementing system-level robustness at component-level (i.e. on-chip) is quickly becoming standard practice, mainly stemming from the desire to reduce system/board design cost. While on paper this may sound as a logical step, it poses enormous challenges to the component ESD Designer in that: 1) IEC 61000-4-2 is NOT applicable to component-level, so every company is struggling to understand/design proprietary characterization methods at component level to extrapolate performance at system-level. 2) ESD Designers are now responsible for the performance of systems they do not build nor, in many cases, they know anything about. In the automotive world, situation is even more challenging. In addition to ESD immunity at system-level, there is a plethora of other requirements against immunity to Electrical Disturbances and immunity to RF disturbances that must be met. This talk will address the ESD Design challenges stemming from automotive system-level ESD specs, along with the trade-offs between ESD Design and EMC Immunity requirements.

Keynote & Invited Speakers



Dr. Charvaka Duvvury
iT2 Technologies

Talk Title: Exploring Machine Learning for ESD Data Analysis

Abstract: Can Machine Learning (ML) take us into greater efficiency of IC ESD Evaluation? What we now know of machine learning has taken on a wide interest in the semiconductor industry. One prime area of exploration of ML would be in ESD data characterization and analysis. This seminar will present ML opportunities for ESD from I-V curve data interpretation for HBM and CDM evaluation to possible applications with TLP and VfTLP data investigations for design purposes. A case study on how IV curve data was analyzed to demonstrate the concept of machine learning to recognize patterns and the potential for predictability from new data on new sets of devices from measurements. Finally, the talk will outline future opportunities of ML in ESD applications.

Prof. Elyse Rosenbaum
University of Illinois Urbana-Champaign

Talk Title: ESD Design for High-speed Wireline IOs in Advanced CMOS Technologies

Abstract: Wireline data rates have reached tens and even hundreds of Gb/s. In each new process technology, it is necessary to develop highly-efficient ESD protection devices, which can safely shunt a large current per unit of (parasitic) capacitance. It is also necessary to jointly optimize the front-end circuitry both for signal integrity and ESD reliability, an endeavor that requires extensive circuit simulations. ESD over-design is not feasible for high-speed IOs and thus the accuracy of the ESD simulations is paramount. Unfortunately, the compact models included in a PDK are not accurate at ESD current levels. Furthermore, the ESD current has a very high slew rate, and an RC extracted netlist will not capture the inductive voltage drops. This presentation will demonstrate that ESD models enable the design of reliable high-speed IO circuits.

Keynote & Invited Speakers

Prof. Mayank Shrivastava
Professor, Indian Institute of Science, Bangalore

Talk Title: Predictive TCAD-Based ESD Design without Foundry Data

Abstract: In the realm of ESD device engineering in advanced and technologically complex nodes, the ability to predict and design robust ESD protection concepts is paramount. Traditional ESD design approaches often rely heavily on foundry-specific data/process information, which can be a limiting factor in terms of accessibility and flexibility. This talk presents an innovative methodology that leverages Technology Computer-Aided Design (TCAD) simulations to predict ESD performance without the need for proprietary foundry/process data. We will delve into the principles and advantages of TCAD-based modeling, demonstrating how these simulations can accurately replicate physical phenomena and predict device behavior under ESD stress conditions. The discussion will cover the integration of predictive modeling techniques, parameter extraction, and the calibration of TCAD models to achieve high-fidelity results. By eliminating the dependency on foundry/process data, this approach not only democratizes ESD design but also accelerates the development cycle, enabling designers to quickly iterate and optimize ESD protection solutions.

Dr. Matteo Buffolo
University of Padova - Department of Information Engineering, Italy

Talk Title: Robustness of GaN-based LED against EOS events and ESDs

Abstract: Over the last twenty years, the reliability of GaN-based visible LEDs has vastly improved, mostly due to optimizations in device structure and in the epitaxial growth, to a point where a useful lifetime of the solid-state source in excess of tens of thousands of hours can be achieved. For these mature devices, extrinsic factors, such as EOS and ESD events, represent a major lifetime-limiting factors during operation on the field. This talk investigates from a physical standpoint the impact of overstress events on GaN-based LEDs, and reports on the device-level mitigation strategies that can be adopted to improve LED robustness against such phenomena.

Dr. Teruo Suzuki
Socionext Inc

Talk Title: Consideration based on ESD applied waveform in High-Speed IF using T-Coil

Abstract: The T-Coil is one of the indispensable circuits in high-speed IF circuits and can reduce the effect of parasitic capacitance in ESD protection circuit. We fabricated a TEG equipped with ESD protection circuit, using the T-Coil driven by the state-of-the-art CMOS technology and investigated its performance. CDM failed at about 3.5A, VF-TLP failed at 2.2A, and the simulation reproduced those measurements. The effect of T-Coil mutual induced voltage is particularly pronounced in VF-TLP and is inconsistent with CDM. Since VF-TLP (TLP) is a tool for ESD design, ESD designers should consider this finding especially for leading-edge CMOS technology processes. There have been some reports of miscorrelation between TLP and ESD measurements, and the T-Coil is yet another case.

Dr. Dolphin Abessolo Bidzo
NXP Semiconductors, The Netherlands

Talk Title: Electronic Design Automation (EDA) Layout Verification Methodology for Charged Device Model (CDM)

Abstract: ESD Electronic Design Automation (EDA) verification tools have become instrumental to the design and verification flow of integrated circuits (IC's). This trend has been mostly driven by the extraordinary development and increasing complexity of IC's in the past few years. With the downscaling of the process technology nodes, CDM represents the main ESD threat for IC's in assembly lines. Furthermore, increasingly demanding product performance with necessary ESD reliability requirements make it very challenging to achieve first-time-right silicon for both functional and ESD exigency. In that context, the use of ESD verification tools to de-risk IC designs before tape-out or for debugging purpose has become critical. ESD verification is not limited to circuit topology analysis. In order to improve its coverage, further geometrical, layout-based checks and simulations are required to verify the proper construction and implementation of ESD protection devices. Complementary to the topological ESD checks, these CDM layout simulations are meant to identify weak ESD paths, to perform a detailed analysis of back-end metallization and to spot victim devices (e.g. gate oxide of MOS devices) exceeding breakdown voltages under CDM like circumstances. The layout verification for CDM is performed at full chip level typically. In this presentation, the methodology of the state of the art CDM layout simulations tools is described, real life case studies are presented and the outlook towards future developments is discussed.

Dr. Kranthi Nagothu
Texas Instruments

Talk Title: On-chip protection Design Challenges for system level ESD

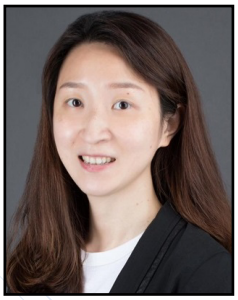
Abstract: In this presentation, unique failure mechanisms in high voltage Silicon Controlled Rectifiers (SCR) under IEC stress are discussed. In one case, the presence of a common mode choke in the stress path was found to change the current waveform shape that the electrostatic discharge (ESD) protection device experiences on-chip. Minor variations in the stress current waveform shape for specific IEC stress levels are found to cause an unexpected window failure in DeNMOS based SCR. In second, Air-Discharge IEC failure in Bi-Directional SCRs that are sensitive to IEC measurement conditions via the pulse rise time are investigated. 3D-TCAD simulations are used to develop the physical Insights of the failure and propose the device level engineering solutions to mitigate the IEC failures.

Keynote & Invited Speakers

Christopher Almeras
Raytheon, an RTX Business

Talk Title: Risk Mitigation in Manufacturing of High Reliability Products

Abstract: Electronics manufacturing is the engine that keeps the world's motor running. Designs of circuit cards and devices continue to become more complex and provide greater power and capabilities to everything we depend on. As the complexity increases, so does the requirements to protect these devices from ESD during manufacturing. When you have product that must work every time, further care needs to be taken to ensure the product is protected throughout the build cycle. In this presentation, we will discuss how the ESD TR19 document on Protection of High Reliability parts, builds on the foundation provided by ANSI/ESD S20.20 to provide further risk mitigation. We will also help answer questions regarding appropriate application and implementation strategies.



Ms. Yang Yanjing
ThermoFisher Sci/Singapore

Talk Title: Failure Analysis workflow for Advanced Packing and Power Semiconductor Device

Abstract: As semiconductor packaging evolves with technologies like 3D-IC, 2.5D, and wafer-level packaging, new reliability and performance challenges emerge, such as die-level defects, TSV formation issues, and bonding problems. Identifying these faults is crucial yet complex, requiring advanced techniques for rapid, precise, and accurate data. This talk will delve into the failure analysis workflow for advanced packaging and power semiconductor devices. It will cover process metrology, characterization challenges, and industry-leading workflows for assembly failure isolation and complete die analysis. Emphasizing techniques for high sample throughput, high resolution, and unmatched automation, the presentation will showcase how to accelerate failure analysis and reduce time-to-data, enhancing device performance, reliability, and yield.

Mr. Mototsugu Okushima
Renesas Electronics, Japan

Talk Title: Efficient CDM Protection Design for Cross Power Domain of Analog/RF block in Finfet Technology

Abstract: Analog/RF circuit blocks that need noise isolation from digital block or each other are increasing more. To protect the vulnerable transistor in finfet technology, power clamp between cross domain is useful. However, increasing number of isolated blocks costs large area for the ESD clamps. To suppress the area increase, this presentation gives an efficient CDM protection design for cross-domain interface circuits especially using "internal cross clamp" as voltage divider between the internal power supply node of analog circuits and the digital GND node. The proposed protection circuit meets high CDM current request from large package IC with finFET technology while suppressing the area increase for analog/RF circuit blocks.

Keynote & Invited Speakers

Dr. Hossam Sarhan
Siemens EDA, France

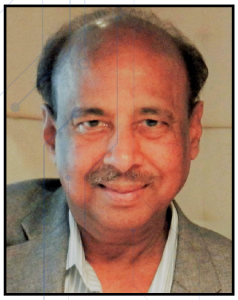
Talk Title: Ensuring Sign-off Design Reliability: Navigating Complex Requirements using Calibre® PERC™

Abstract: Conservative design rules and constraints are often used in reliability verification flows. Foundry qualified and supported rule decks, augmented by custom checks, are essential to establishing this reliability baseline, not only to guide improvements, but also to establish best practices with internal and 3rd party IP through full-chip sign-off. When verifying the robustness of your electrostatic discharge (ESD) protection strategy in your design, it is essential to ensure sufficiently sized devices and interconnects while understanding ESD margins with SPICE-accurate full-chip simulation.
The Calibre PERC reliability platform automatically combines netlist and layout information to perform targeted electrical checks that consider the context of the design intent for both layout-related and circuit-dependent checks. We will explore exciting challenges and verification developments to ensure reliability in your designs.

Prof. David Pommerenke
Institute of electronics, Graz university of technology, Austria

Talk Title: System Efficient ESD Design

Abstract: This talk discusses the protection of I/O from ESD. In the past, transient voltage protection could be selected from a data sheet. However, the shrinking of the design window due to smaller IC feature size combined with data rates > 50 Gbit/sec forces design by simulation. The system efficient ESD design process creates models of the TVS and the IC. In combination with passive components or traces, a complete model is created that allows ESD robustness to be predicted. The talk will explain the overall process, the measurement techniques used to gather the data needed for modeling, and the models themselves. It will show the capabilities and limitations of these methods and enable the audience to follow the process.



Dr. Charvaka Duvvury
iT2 Technologies

Talk Title: Green ESD: Efficient Test Methods to Save Time and Effort During Qualification

Abstract: ESD qualification test methods often consume significant testing times to meet HBM and CDM spec requirements. This is especially the case for products with multiple power domains and/or IC packages with high pin counts. During the last several years improvements have been demonstrated to significantly reduce testing times by employing more efficient test methods which have been approved by JEDEC. This seminar will review these methods that include novel sampling approaches for cloned IO pins as well as outlining techniques for avoiding misleading interpretation of CDM data often resulting in cumulative effects. The seminar will conclude with an outlook into more advanced statistical methods.

Anamika Chowdhury
Lam Research

Talk Title: Low Pressure Reactor Design to Avoid Unwanted Electrostatic Discharge

Abstract: Arcing, which is one form of Electrostatic discharge, is a common phenomenon in plasma equipment, especially between components which have high potential difference or charge density. While arcing has many industrial applications including welding and combustion processes, unwanted arcing happening at and above the electrical breakdown voltages can result in equipment damage and yield loss. Initial efforts focused on experimentally recording breakdown voltages under applied RF fields for a range of gases and electrode geometries [1-3]. Kihara [4] gave a kinetic treatment of processes occurring in RF electrical discharges in gases and obtained a condition for gas breakdown, which was further validated by Lisovskiy and Yegorenkov [5]. Recent research has focused on using Particle-In-Cell (PIC) simulations to improve agreement between theoretical and experimentally recorded Paschen curves [6-7].
In this talk, we will highlight the past scientific developments in calculation of breakdown voltage. Using a simplified plasma reactor geometry as an example, we demonstrate how reactor design is modified to eliminate arcing risk.

References

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2. Thomson J 1937 Phil. Mag. 23 1
3. Chenot M 1948 Ann. Phys., Paris 3 277
4. Kihara T 1952 Rev. Mod. Phys. 24 45
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6. Wu H 2021 Plasma Sources Sci. Technol. 30 065029
7. Puač M 2018 Plasma Sources Sci. Technol. 27 075013

Mr. Anurag Mittal
Synopsys

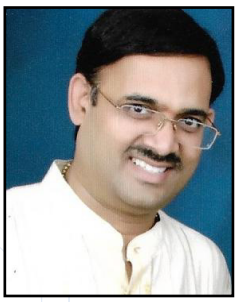
Talk Title: I/O ESD implementation for 2.5D/3D Applications

Abstract: Multi-Die implementations require thousands of short communication I/O channels to drive and receive data. The channel is formed over an interposer, between dices that are in close proximity. It creates an imperative need for a fast and reliable integration of the Die 2 Die interface IOs in the 2.5 D/ 3 D design flow. Conventionally I/Os and ESD cells are Analog macros and need manual cluster-based placement in SoC design flow. We shall discuss in our presentation how our simplified offer caters to all these design challenges. Moreover, conventional CDM architectures may not be suitable for D2D implementations due to large area, cap and leakage constraints. We evaluate few conventional versus novel CDM architectures to meet high density multi-die I/O ESD implementations.

Mrs. Chinmayee Panigrahi
NXP Semiconductors

Talk Title: Challenges in ESD protection for High Speed CML transmitter having thin oxide devices and their solution

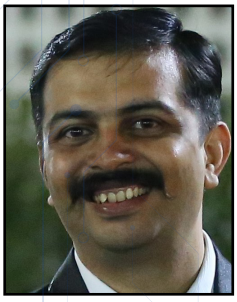
Abstract: ESD protection of High-Speed PADs is very challenging as ESD elements add capacitance to PAD which limits the max frequency of operation. This talk presents the challenges in ESD protection of CML transmitter for 5.5GHz Clock and 5.5 Gbps data in 0.9V Signaling, done in CLN28HPCP technology using thin oxide (GO1) devices. Ensuring sufficient ESD robustness for GO1 devices is difficult as protection circuit shall shunt the ESD current and keep the voltage drop below the failure voltage of GO1 devices. Conventional ESD strategy of direct ESD protection between differential PADs limits the bandwidth. An innovative ESD solution is used for achieving 5.5GHz frequency and at the same time achieving the ESD robustness.



Dr. Dattatreya Prabhu Rachakonda
GlobalFoundries

Talk Title: Learnings from Switch Self-Protection : from models to hardware

Abstract: The Switch is an integral component of any communication front end module. The configurations like Single Pole Double Throw (SPDT) employ a series-shunt combination of Mosfets (SwitchFETs). Being large devices (say >1mm in width) the devices are expected to self-protect from possible ESD events. This talk will aim to decipher the physics behind the ESD performance of the silicided SwitchFETs both at the device level as well as in the switch-stack configuration. Efforts to ascertain and replicate the observed failure current trends using TCAD and capture the geometric and bias dependence in a compact model will be highlighted. As a next step the performance of the compact model in predicting the transient behavior of the switch-stack vs. hardware will also be outlined.



Mr. Harshit Dhakad
Intel Technologies India Pvt

Talk Title: Tracing and debugging of ESD failures in a module assembly line

Abstract: His current work focusses on development of RF & high speed interface ESD protection concepts & ESD verification methodology for complex SoC's ESD Testing Tracing and Debugging of ESD Failures in a Module Assembly Line A functional failure of a connectivity module is investigated and traced down to transistor level in the CMOS IC. The presentation discusses failure analysis, layout inspection, ESD simulations, ESD test experiments to validate and understand the root cause and process assessment in the assembly line. The analysis identified a charged board event as the issue.

Gopikrishna Siddula
Western Digital

Talk Title: Enhancing Reliability in High speed and High-Density Storage: Practical Strategies for Mitigating Electrostatic Discharge (ESD)

Abstract: Electrostatic Discharge (ESD) poses significant challenges to the reliability of high-speed and high-density storage systems. This presentation delves into practical strategies for mitigating ESD, focusing on innovative design and engineering solutions. Key topics include the implementation of ESD design approaches for different storage product lines, enhanced resistance analysis, grounding techniques, and optimized circuit designs to minimize ESD vulnerability. This session also covers real-world case studies demonstrating successful ESD mitigation in cutting-edge storage technologies.

Manohar Seetharam
Samsung Semiconductor India Research

Talk Title: A Robust ESD Protection Scheme for High-Speed Serial Interface in 3nm MBCFET Technology

Abstract: Low power wireline circuits have derived substantial benefit from FinFet, GAA and MBCFET process nodes. However, these processes are also more sensitive to ESD events. Simple incorporation of a T-coil was traditionally sufficient to overcome this problem and trade-off with high-speed performance. The proposed ESD methodology and scheme meets greater than 250V & 7A CDM strike while supporting more than 24Gbps speed on the data pins. The design was fabricated in Samsung 3nm MBCFET process and the Silicon performance verified. The paper also discusses the challenge posed by high resistive metal and vias used in the 3nm process.

Mr. Sharath B N
COMSOL

Talk Title: Multiphysics Simulation for the Semiconductor Industry

Abstract: Modeling and simulation of semiconductor devices, their manufacture, and the components and infrastructure surrounding them has become more complex due to a number of factors, such as the reduction in the size of semiconductor devices, the general competitiveness of the industry, and requirements for increasing their performance. The ability to accurately model these devices and associated manufacturing technology increasingly requires a multiphysics approach to define and analyze their physical aspects. COMSOL Multiphysics®, along with its add-on products, have been widely used for design and optimization in semiconductor processing. Join us in this session to learn more about the use of multiphysics simulation for the modeling and simulation of semiconductors and semiconductor processes. The speaker will also discuss the role of multiphysics simulation in electrostatic discharge applications and thermal management of electronics.

Ph.D. Research Talks

Monishmurali M (Indian Institute of Science)

Talk Title: Addressing design challenges for current uniformity in Fin-based SCRs

Abstract: This talk presents advancements in designing Fin-based Silicon-Controlled Rectifiers (SCRs) for ESD protection, focusing on addressing critical challenges in ESD current localization, failure current scalability, and current filament formation. It explores tap engineering techniques to improve conduction uniformity across anode and cathode junctions. These techniques include various n-Tap and p-Tap configurations, leading to the development of new Fin-based SCR schemes. Additionally, 2D and 3D current filament dynamics within these SCRs are discussed, highlighting enhancements in turn-on uniformity and filament spreading dynamics. These findings promise significant improvements in SCR performance and reliability under ESD stress.

Rasik Rashid Malik (Indian Institute of Science)

Talk Title: Interplay of Surface Passivation and Electric Field Distribution in Determining ESD Behaviour of p-GaN Gated AlGaN/GaN HEMTs

Abstract: This paper presents the dependence of ESD robustness on the electric field distribution in p-GaN gated HEMTs. The Al% in the bilayer AlxTi1-xO/SiO2 passivation is used as a tuning parameter to modulate the electric field distribution. It was observed that the ESD robustness of the devices increased as the electric field intensity near the gate edge decreased. Two distinct failure modes related to the electric field distribution were identified through leakage behavior, electroluminescence microscopy, Raman spectroscopy, and SEM imaging of ESD-damaged devices. Devices with higher electric field peaks near the gate edge exhibited tensile stress buildup in the gate-source access region, leading to a sudden rise in TLP leakage at snapback and gate-driven failures. Conversely, devices with lower electric field peak intensity showed compressive stress buildup in the gate-source and gate-drain access regions, a gradual increase in leakage after snapback, and are susceptible to drain-to-source driven failure mechanism.

Mitesh Goyal (Indian Institute of Science)

Talk Title: Load-line Dependent Current Filament Dynamics in Nanoscale SCR Devices

Abstract: In this presentation physics of experimentally observed abnormal behavior in STI bounded Silicon-Controlled-Rectifier (SCR) structures is investigated and explained using basic principles and 3D electrothermal TCAD simulations. The device physics during ESD event is thoroughly simulated and the behaviour is observed. The SCR device is found to show pulse to pulse instability in the negative resistance (snapback) region during the 100ns pulse width TLP measurement. The instabilities were independent of SCR geometrical design variations but were dependent on the load line conditions used in the TLP measurement. The physical insights and device physics has been explored using well calibrated 3D process and device TCAD.

Mohammad Ateeb Munshi (Indian Institute of Science)

Talk Title: Understanding Temperature Dependence of ESD Reliability in AlGaN/GaN HEMTs.

Abstract: In this work we report the role of temperature on the ESD reliability of AlGaN/GaN HEMTs, emulating a system level scenario. We compared two stacks with different carbon doping concentration, LC (low carbon doping) and HC (high carbon doping). The trigger voltage (Vtr) was seen to decrease with increasing temperature in LC, while as Vtr remained independent of the temperature for HC. The modulation of field due to the temperature is seen to govern the ESD behavior of the LC. While as in HC, hot holes due to avalanche and hole emission in the high carbon doped buffer determine the breakdown behavior. This study shows the need of an optimum buffer to ensure the ESD robustness of AlGaN/GaN HEMTs with temperature.

Custom ESD Protection for 10 V - Compliant Neural Stimulators in 65nm CMOS Technology.

Naef Ahmad, Tanay Das, Navin Maheshwari, Sandip Lashkare, Laxmeesha Somappa
(IIT Bombay, IIT Gandhinagar)

Abstract: Implantable neurostimulators use internally generated high-voltages (up to 10V) to suppress seizures using a pair of electrodes. For such applications, traditional foundry provided ESD protection is inadequate due to such custom voltage requirements. Here, a pair of diodes is proposed as a custom ESD protection verified using schematic simulations (TSMC 65nm) with an HBM model. The diode structure's 2D layout is simulated in TCAD for TLP measurements to identify local temperature hotspots by current crowding and failure currents. Finally, multiple diode fingers are then implemented to distribute ESD current uniformly, reducing footprint and dynamic resistance, meeting the custom voltage requirement.

ESD Solution for Die-to-Die I/Os.

Bhawana Adhikari **(Synopsys)**

Abstract: Explore the future of semiconductor packaging with our insights into 2.5D and 3D technologies, featuring advanced Interposer and Silicon Interconnect solutions. While conventional IOs are familiar with ESD risk and solution, the emerging D2D IOs require a fresh outlook to meet IP ESD requirements with optimum area and performance impact. This poster will include detailed insight of our current offer in D2D IO and ESD solution implementation and will share how ESD solutions are made compatible with standard cell logic for seamless implementation of thousands of IOs with required ESD protection in digital flow.

Cross-Domain menace in an IO Cluster.

Siddharth Singh **(Synopsys)**

Abstract: The modern chips are moving to a single ground throughout the chip. Does it mean that the long-standing perilous event of cross-domain ESD has been solved? The cross-domain interface circuits can easily be damaged during cross-domain ESD events. Due to CDM charges distributed throughout the entire chip, charges need an effective cross-domain ESD path to discharge during an CDM event. In this study we analysed various cross-domain solutions which have been followed traditionally and recommended by the foundries. We analysed the significance of having an Anti-parallel diode between to separate ground domains alongside the impact of routing resistance of these diodes. Additionally, how having a dedicated cross-domain clamp mitigates the risk significantly. Lastly, we will discuss how having a single ground throughout the chip helps during ESD event. But does it mean we can overlook the cross-domain issue if we have single ground? The answer is NO. We will be discussing it with an intriguing cross-domain failure that we tackled on our Si testchip.

Adaptive ESD Protection Circuits: A Dynamic Approach to Enhancing Chip Reliability.

Abishekkumar A (Anna University)

Abstract: Electrostatic Discharge (ESD) is a major challenge in integrated circuit (IC) design and manufacturing. Traditional ESD protection methods lack flexibility for varying threats. This paper introduces Adaptive ESD Protection Circuits, which adjust protection mechanisms in real-time based on detected ESD events. Using smart sensing technologies and advanced algorithms, these circuits optimize protection while minimizing impact on normal operation. We discuss design principles, implementation challenges, and benefits over conventional methods. Case studies highlight significant improvements in ESD resilience and reliability, demonstrating the potential of adaptive ESD protection for future semiconductor designs.

Embedded Passives in Advanced Packaging: Enhancing ESD Protection and Circuit Performance

Prathipa L (Anna University)

Abstract: As the demand for miniaturized, high-performance electronics grows, advanced packaging techniques have become crucial. This paper explores the use of embedded passives, such as resistors, capacitors, and inductors, integrated within the chip package. This approach reduces parasitic elements, shortens signal paths, and enhances electrical performance and ESD protection. We highlight the design, fabrication processes, and benefits over traditional components, supported by simulations and experimental results. Case studies demonstrate improved ESD resilience and system reliability. Challenges and future directions in adopting embedded passives are discussed, emphasizing their potential to meet the stringent demands of modern electronics.

Charged Device Model Testing for the future.

Thomas Meuse (Thermo Fisher Scientific)

Abstract: More ESD related failures are occurring during manufacturing process, so testing devices to events such as those emulated by the Charge Device Model (CDM) test is becoming more important! The field-induced CDM method in ANSI/ESDSA/JEDEC JS-002 is widely used, however there are issues with this method, due to the air discharge created when initiating the discharge. One issue is the variation of the pulse amplitude, which becomes even more variable as the pre-charge voltage decreases. A contact method, referred to as low-impedance contact CDM (LI-CCDM) eliminates the air discharge and thereby improves repeatably and reproducibility. This method will be reviewed.

Interplay of Surface Passivation and Electric Field in Determining ESD Behaviour of p-GaN Gated AlGaN/GaN HEMTs.

Rasik Rashid Malik, Avinas N Shaji, Jayshree, Zubear Khan, Madhura, M. A. Munshi, Rajarshi R. Chaudhuri, Vipin Joshi, and Mayank Shrivastava (Indian Institute of Science)

Abstract: Electrostatic Discharge (ESD) is a major challenge in integrated circuit (IC) design and manufacturing. Traditional ESD protection methods lack flexibility for varying threats. This paper introduces Adaptive ESD Protection Circuits, which adjust protection mechanisms in real-time based on detected ESD events. Using smart sensing technologies and advanced algorithms, these circuits optimize protection while minimizing impact on normal operation. We discuss design principles, implementation challenges, and benefits over conventional methods. Case studies highlight significant improvements in ESD resilience and reliability, demonstrating the potential of adaptive ESD protection for future semiconductor designs.

Multifinger Turn-On Instability in Drain Extended Vertically Stacked Nanosheet FETs Under ESD Stress Conditions.

Jatin, M. Monishmurali and M. Shrivastava
(Indian Institute of Science & Currently with Analog Devices)

Abstract: A multifinger drain extended (DE) nanosheet FET has been studied for its multifinger turn-on uniformity under electrostatic discharge (ESD) stress conditions using 3-D TCAD simulations. Current and temperature instabilities were seen in the multifinger devices under high current transmission line pulsing (TLP) stress. These instabilities, which may result in premature device failure, were found to be attributed to nonuniform finger turn-on. The physics of nonuniform turn-on in multifinger devices has been probed and on the basis of the observations drawn from the physical insights developed, novel extension fin engineering guidelines have been proposed to mitigate the nonuniform finger turn-on.

Origami method in ESD Packaging.

Ganesh T N Bhushan (JAIN University)

Abstract: The proposal of including origami in sustainable packaging is a surplus note on technological advancement. Specially from SIT, Japan, wherein a decade long emphasis of utilitarian amalgam of origami in minuting the space and enhancing packing efficiency is subjected to industrial mechanisms and machinery, But concerned to that of Electro-Static Devices, the tryst of adaption and implement could make a greater move for revolutionary remarks on ESD packaging. Currently, project proposals on implementing suitable paradigm methods of simulation and algorithm on MoC, design patterns and pain-points are focused under laboratory and working conditions of ESDs & piezo-static instrumentation, concerning to eradicate hazards and cautions.

Load-line Dependent Current Filament Dynamics in Nanoscale SCR Devices.

Mitesh Goyal, Mukesh Chaturvedi, Raju Kumar, Mahesh Vaidya, Mayank Shrivastava
(Indian Institute of Science & Samsung Semiconductor India Research)

Abstract: In this work physics of experimentally observed abnormal behavior in STI bounded Silicon-Controlled-Rectifier (SCR) structures is investigated and explained using basic principles and 3D electrothermal TCAD simulations. The SCR device is found to show pulse to pulse instability in the negative resistance (snapback) region during the 100ns pulse width TLP measurement. The instabilities were independent of SCR geometrical design variations but were dependent on the load line conditions used in the TLP measurement. The physical insights and device physics has been explored using well calibrated 3D process and device TCAD.

Missing Trigger Circuit Action and Device Engineering for Conventional Nanoscale SCR.

Mitesh Goyal, Mukesh Chaturvedi, Raju Kumar, Mahesh Vaidya, Mayank Shrivastava
(Indian Institute of Science & Samsung Semiconductor India Research)

Abstract: In this work co-optimization of silicon-controlled rectifier (SCR) ESD characteristics with its low voltage trigger circuit is presented. Resistance and Capacitance (RC) controlled thick gate NMOS and PMOS based circuits have been explored and compared. The design approach is discussed and presented for low trigger SCR for two different trigger circuits. In the process we find that some of the trigger circuits previously reported in literature do not work as desired until co-optimized device engineering techniques are used. The circuit insights are explored using well calibrated electrothermal 3D process and device TCAD mixed mode simulations.

Current Scalability Issues in Multi-Bank 5V PMOS ESD structures: Root cause and Design Guideline.

Kranthi Nagothu, Yang Xiu, Yang Xiao, Rajkumar Sankaralingam (Texas Instruments)

Abstract: In this work, a unique Human Body Model (HBM) failure is presented in 5V-PMOS multi-finger structures. The failure is sensitive to the multi-bank layout, generally used to achieve higher holding voltage. Missing Transmission Line Pulse (TLP) failure current (It2) scalability is detected with pulse width, in multi-bank structures and a correlation is established with lower HBM failure. A detailed 3D-TCAD analysis approach is used to understand the PMOS turn-on in the singlebank and multi-bank structures, in turn, the It2 scalability for longer pulse width. The obtained insights are used to provide design guidelines for developing robust PMOS devices.

Understanding Temperature Dependence of ESD Breakdown in AlGaN/GaN HEMTs.

Mohammad Ateeb Munshi, Mehak Ashraf Mir, Vipin Joshi, Rajarshi Roy Chaudhuri, Zubear Khan, Mayank Shrivastava (Indian Institute of Science)

Abstract: In this work, we report the role of temperature on the ESD reliability of AlGaN/GaN HEMTs emulating system-level scenario. We compared two stacks with different buffer carbon doping concentration, LC (low carbon doping) and HC (high carbon doping). The failure voltage (Vbd) was seen to decrease with increasing temperature in LC, while Vbd remained independent of the temperature for HC. The modulation of electric field due to the temperature is seen to govern the ESD behavior of the LC. Inverse piezoeletric effect governs the breakdown in LC, while, as in HC, hot holes due to avalanche and hole emission in the high carbon doped buffer determine the breakdown behavior. This study shows the need of an optimum buffer to ensure the ESD robustness of AlGaN/GaN HEMTs with temperature.

Impact of a Deep Junction Coupled with a Short Channel Length on the ESD Robustness of a Grounded Gate NMOS Clamp.

Casey Hopper, Antonio Gallerano, Raj Sankaralingam
(Advanced Technology Development, Texas Instruments Inc.)

Abstract: Several physical insights into the multi-finger turn-on in deep junction GGNMOS devices and its implication on eventual failure current is presented with detailed experiments. The impact of junction depth to channel length ratio is found to be a key design factor in obtaining ESD robustness.

Engineering Custom TLP Characteristic Using a SCR-Diode Series ESD Protection Concept.

Harsha B Variar, Satendra Kumar Gautam, Ashita Kumar, Amogh K M, Juan Luo, Ning Shi, David Marreiro, Shekar Mallikarjunaswamy and Mayank Shrivastava
(Indian Institute of Science and Alpha & Omega Semiconductor)

Abstract: This work demonstrates an SCR-Diode series ESD Protection concept, which can be engineered to provide a custom TLP I-V characteristic. SCRs and diodes with dimensional variations have been used in different combinations and width ratios, which results in a range of TLP I-V characteristics. This protection circuit comes with several advantages as adaptability for various ESD protection windows, the benefits of using SCR as a protection device and the ease of designing the circuit. Along with TCAD studies, experimental data demonstrates that N-well and P-well doping of SCR can be used to further tune the Vhold and Ron of the protection circuit.

3D Approaches to Engineer Holding Voltage of SCR.

Suruchi Sharma, Satendra Kumar Gautam, Harsha B Variar, Juan Luo, Ning Shi, David Marreiro, Shekar Mallikarjunaswamy, Mayank Shrivastava
(Indian Institute of Science and Alpha & Omega Semiconductor)

Abstract: Novel Silicon-Controlled-Rectifier (SCR) structures are experimentally demonstrated with the cathode and anode region engineering in the width (3D) plane. The engineering approach uses unique placements of P+ and N+ pockets/strips, instead of uniform anode/cathode implants. Experimental results show tunable holding voltages (3V - 10V) with high ESD failure current (It2) by using layout parameters related to the placement of these pockets/strips. The same has been demonstrated for over a dozen process lots. The physical insights and engineering guidelines into the holding voltage tuning has been explored using 3D process and device TCAD.

High-Performance LDMOS-SCR with Improved ESD Robustness.

Monishmurali M (Texas Instruments)

Abstract: Conventional LDMOS-SCR devices were improved to enhance their DC performance without flipping the anode side contacts. This was achieved by studying the PNP, NPN, and SCR triggers under DC operational conditions. NPN engineering was also investigated using TCAD to prevent failure during normal DC operation while maintaining the PNP action. A 72% increase in the maximum drive current was achieved on silicon by degrading the NPN alone and retaining the PNP action. Finally, the RF performance of all the variant of LDMOS devices are
presented.

Effect of Source & Drain Side Abutting on the Low Current Filamentation in LDMOS-SCR Devices.

Monishmurali M, Kranthi Nagothu, Gianluca Boselli, Mayank Shrivastava (Texas Instruments)

Abstract: The concept of abutting source/body and drain/anode junctions is studied in detail in a high voltage LDMOS-SCR with 2D and 3D TCAD simulations. The SCR turn-on and low current filament formation are strongly influenced by the isolation at the anode and cathode side in the LDMOS-SCR. While the anode side isolation impacts the filament-induced failures at low currents, the cathode side isolation has a minor impact. Physical insights are given on the SCR turn-on degradation with abutting and its influence on the filament formation and spreading. The obtained understanding helps to build an ESD robust, self-protected LDMOS-SCRs.

TI's Discrete Protection Diodes Portfolio with Ultra-Low Capacitance.

Kartikey Thakar (Texas Instruments)

Abstract: Did you know Texas Instruments has dedicated process technology for their discrete protection diodes? This is designed and optimized to achieve top-of-the-class ESD protection while achieving one of the lowest capacitance values for the same class of devices. TI protection diodes are designed to achieve suitable low cap required for slow data rate (a few Kb) to very high-speed data lines (USB2/3 HDMI1/2). In this talk, we discuss a range of external ESD protection solutions offered by TI for both Commercial/Industrial and Automotive applications, suitable for power as well as data lines.

Physics of ESD reliability in amorphous silicon based TFTs.

Rajat Sinha, Prasenjit Bhattacharya, Icko Eric Timothy Iben, Sanjiv Sambandan, Mayank Shrivastava (Micron Technology India, Indian Institute of Science)

Abstract: This work presents the physical behavior of non crystalline silicon based TFTs including dielectric breakdown and thermal failure under ESD Conditions. It also presents a unique phase transition behavior and explores device degradation under ESD Conditions.

Increased ESD robustness of non crystalline silicon based TFTs using novel architectures.

Rajat Sinha, Sanjiv Sambandan, Mayank Shrivastava (Micron Technology India, Indian Institute of Science)

Abstract: This works explores various device architectures that can be used to improve the ESD robustness of non crystalline materials based TFTs. These architectures are shown to have low real estate penalities and need not require additional masks steps.

ESD design methodology for GPIO design.

Dzung Tran, Saleh Omar, Vaibhav Katkar, Prashanth Singh, Mridula Pai, Thiru Ranganathan (GlobalFoundries)

Abstract: Soc Implementations demand robust design flow practices GPIP design. This paper describes an ESD design methodology for GPIO design.

BEOL Optimization of ESD devices for RF application

Sitansusekhar Roymohapatra (GlobalFoundries)

Abstract: Radio frequency (RF) electrostatic discharge (ESD) protection design is emerging as a new challenge to RF integrated circuits (IC) design. Designers are looking towards RFIC-ESD co-design to provide ESD protection devices with minimum possible capacitance. But in advanced node ESD protection devices, the capacitance offered by back-end-of-line (BEOL) is comparable to the front-end-of-line (FEOL) capacitance. The BEOL capacitance optimization is the need of the hour to offer robust HBM and CDM protection without degrading the RFIC performances. This poster reviews different designs for BEOL optimization of ESD protection devices.

ESD protected Isolation cell with low Leakage and complaint to power-aware verification

Pramod Gayakwad, Mukesh Kumar, Jeethu Benny, Gagan Kansal (NXP Semiconductors)

Abstract: To reduce power consumption in chips, designs are partitioned into multiple power-domains, requiring additional circuits, such as Level Shifter, Always-ON and ISOlation cells. Signals crossing power domains need CDM ESD protection circuit and ISO/LS cells. Chip failures occurred when the ESD and ISO circuit connections were incorrectly connected and, in another situation, ESD circuit had an inaccurate timing model issue during System on Chip timing analysis. To resolve these problems, a resilient ESD+ISO macro cell was developed, which is power-aware for SoC design UPF implementation and verification needs, while having low leakage and accurate timing model.

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