InEW 2025
India ESD Workshop

IEEE Advancing Technology for Humanity

CALL FOR POSTER

25th - 26th August 2025

6th India ESD Workshop

Indian Institute of Science, Bangalore, India

India ESD Workshop (InEW)

ESD reliability understanding and how to design ESD safe chips have always been highly important and crucial aspects for semiconductor design, development, testing, and manufacturing cycles. Given the absence of ESD design/testing/technology knowledge, expertise, and awareness in India, in 2015 **Indian Institute of Science (IISc), Bangalore** started efforts for industry professionals and students, which today is called **India ESD Workshop (InEW).** This conference has gathered significant interest and traction from the semiconductor industry professionals in India, with the potential to expand to other regions going forward. For example, the last edition attracted 250+ senior-level engineers from the semiconductor industry. The conference has also flourished due to its significant collaborations with industry leaders like Global Foundries, Samsung, NXP Semiconductors, Texas Instruments, Cadence, Infineon, Western Digital, Intel, Micron Technology, AOS, Synopsys, ST Microelectronics, Qualcomm, etc. The objective of the conference has always been to promote the knowledge, know-how, and expertise in ESD design, technology, and testing, in collaboration with global ESD experts. With the growing manufacturing requirements, manufacturing push in the country, upcoming fabs, an increasing number of chip design centers getting into full product cycles (full product developments), and an increasing number of chip design start-ups with efforts on end products, this expertise becomes more than relevant and justifies the need and growth of venues like InEW to continue and grow. With the current context, it would not be an exaggeration if the conference grows to 500+ professionals in the years to come.

Submission Deadline: June 25, 2025
Notification of Acceptance: June 30, 2025

Submit your Poster Abstract Here

Venue: Indian Institute of Science, Bangalore
Organized By: Prof. Mayank Shrivastava (IISc)

Web: https://iisc-inew.org/
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InEW 2025 India ESD Workshop

Tracks / Technical Focus

- Advanced CMOS: FinFET, Nanowires, Nanosheets, etc: ESD Issues in Advanced Technologies (Multi-gate, FinFET, SOI, SiGe, nanowire, etc.), On-Chip ESD Protection Devices and techniques in Advanced CMOS Technologies, IC Design and Layout Issues, Circuit Simulation of EOS/ESD Events in Advanced CMOS Technologies, DC/Transient Latch-up Issues and Solutions.

- Emerging Technologies: 2D, RRAM, Neuromorphic Devices, Quantum, etc: ESD issues in novel devices with the 2D layered semiconductor or dielectric materials, logic, and memory devices, neuromorphic devices, quantum devices and quantum-enhanced technologies

- 2.5D & 3D Stacking, TSV, Backside Power Delivery Network: ESD Issues and solutions in 2.5D & 3D IC packaging and integration, interconnects, TSV, ESD protection requirements in Backside Power Delivery Network

- Analog & Automotive Technologies: Bipolar, RF, High Voltage, and BCD: ESD Issues, on-chip ESD protection devices and techniques, IC Design and layout issues, ESD circuit simulation and co-design, DC/Transient Latch-up Issues and Solutions in Bipolar, RF, High Voltage, and BCD Technologies

- ESD Testing: ESD Testing trends with Technology Scaling; Multi-dimensional packaging; ESD Test and Characterization method; Traditional and Novel TLP Testing System; HBM and CDM testing issues and solutions; Reliability Test equipment; New failure mechanism; Advanced failure analysis techniques; ESD Checking and verification Technology.

- ESD Device & System Modelling: System level Test, modeling and simulation method; Circuit level design and simulation of ESD Events in Advanced CMOS Technologies; Use of EDA tools; IC Design and Layout issues; Transient ESD induced upset; Robustness evaluation for standard test boards; Large scale analysis with machine and deep learning.

- Numerical Modeling and Simulation of ESD Components: Component level ESD design including but not limited to SCR, LDMOS, GGNMOS, GDPMOS, Diode, etc.; TCAD/Circuit Simulation; Numerical modeling and Physics of ESD events; Advanced simulation technologies (SOI, SiGe, FinFET, Compound, Nanowire); Latchup detection prevention and mitigation; Simulation tools and methodology

- ESD CAD & Verification: ESD modeling, design guidelines, testing standards, whole chip ESD protection, design verification, compliance testing, ESD Protection for mixed voltage applications.

- System Level ESD: System efficient ESD design (SEED), ESD testing standards (IEC), co-design methodology of on-board and on-chip ESD protection, ESD protection for consumer electronics, automotive, aerospace, and industrial applications.

- ESD and EOS Protection in GaN HEMTs & GaN Power ICs: GaN technology-based ESD protection diodes, TVS, testing and shielding techniques, EOS protection from overvoltage conditions, current surges, and power supply instability.