InEW 2026
India ESD Workshop

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7th - 8th September 2026

7th India ESD Workshop

Indian Institute of Science, Bangalore, India

TECHNICAL PROGRAM

Venue: Indian Institute of Science, Bangalore
Organised By: Prof. Mayank Shrivastava (IISc)

Web: https://iisc-inew.org/
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InEW 2025 India ESD Workshop

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About the India ESD Workshop (InEW)

ESD reliability understanding and how to design ESD safe chips have always been highly important and crucial aspects for semiconductor design, development, testing, and manufacturing cycles. Given the absence of ESD design/testing/technology knowledge, expertise, and awareness in India, in 2015 **Indian Institute of Science (IISc), Bangalore** started efforts for industry professionals and students, which today is called **India ESD Workshop (InEW).** This conference has gathered significant interest and traction from the semiconductor industry professionals in India, with the potential to expand to other regions going forward. For example, the last edition attracted 250+ senior-level engineers from the semiconductor industry. The conference has also flourished due to its significant collaborations with industry leaders like Intel, Samsung, Texas Instruments, Western Digital, Global Foundry, Qualcomm, Synopsys, Cadence and NXP etc. The objective of the conference has always been to promote the knowledge, know-how, and expertise in ESD design, technology, and testing, in collaboration with global ESD experts. With the growing manufacturing requirements, manufacturing push in the country, upcoming fabs, an increasing number of chip design centers getting into full product cycles (full product developments), and an increasing number of chip design start-ups with efforts on end products, this expertise becomes more than relevant and justifies the need and growth of venues like InEW to continue and grow. With the current context, it would not be an exaggeration if the conference grows to 500+ professionals in the years to come.

Poster Session

An interactive Poster Session of 30 plus posters with High Tea. Participants get to see a variety of world class research done in the area of Electrostatic discharge and get to ask questions and engage in dialogue with the presenters.

Meet World Renowned Experts

A platform for poised to revolutionize the way industry leaders connect with top-tier talent. Our platform ensures that every expert in the field of Electrostatic Discharge is showcased to potential collaborators and employers on a global scale.

Industry Sessions

Heated and seated discussion sessions, in a relaxed setting, on emerging technological areas or key showstoppers or major scientific debates with a quest to find the role academia must play in the next 10 years.

Panel Discussion

To brainstorm on the major ESD induced bottlenecks in the cutting edge technologies and products in the Semiconductor Industry.

Industry Interaction

Conducting collaborative brainstorming sessions to explore opportunities for closer engagement with the industry. This initiative aims to establish a distinctive platform for fostering robust academia-industry partnerships, culminating in the development of a comprehensive 10-year plan and roadmap.

Young Researchers Meet

A special session to explore research opportunities in leading R&D Labs and academic institutions in India.

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Workshop Highlights

03	Keynote Talks	01	Panel Session
30+	Technical Talks	10	Platform Presentations
20+	Poster Presentations	250+	Attendees

Why Attend and Participate?

- Global Engagement: Collaborate with international ESD design experts, resolving design complexities and pioneering resilient ESD design and protection strategies.
- Cutting-edge Discoveries: Dive deep into innovative process technologies, gaining insights into their global implications and applications.
- Expansive Networking: Connect with global peers, industry leaders, and academics, establishing valuable partnerships for the future.
- Present and Propel: Showcase your work on a global stage, attracting diverse perspectives, accolades, and potentially setting industry standards.
- For Students: A unique platform to learn, shine, and perhaps, chart a future course with potential employers from across the globe.
- Relevance to the Global Community: At a time when electronic intricacies intersect with the demand for robustness and reliability, understanding ESD challenges is not just essential; it's critical. InEW-2026 promises to be the crucible where knowledge meets application, innovation meets industry, and challenges meet solutions. It aims to not only address current ESD challenges but also proactively envision and counter future hurdles, ensuring the global VLSI community stays ahead of the curve.

As we stand on the cusp of technological revolutions, with semiconductor technologies reaching their fundamental limits, and devices becoming smarter and more interconnected, the significance of ESD reliability cannot be overstated. Join us at India ESD Workshop 2026. Be part of this global movement, shaping the trajectory of On-Chip and System level ESD design and reliability physics in the realm of a plethora of semiconductor technologies. Together, let's drive a global ESD knowledge renaissance for a technologically resilient future.

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Topics of Interest

1. Advanced CMOS: FinFET, Nanowires, Nanosheets, etc.

ESD Issues in Advanced Technologies (Multi-gate, FinFET, SOI, SiGe, nanowire, etc.), On-Chip ESD Protection Devices & Techniques in Advanced CMOS Technologies, IC Design and Layout Issues, Circuit Simulation of EOS/ESD Events in Advanced CMOS Technologies, DC/Transient Latch-up Issues and Solutions.

2. Emerging Technologies: 2D, RRAM, Neuromorphic Devices, Quantum, etc.

ESD issues in novel devices with 2D layered semiconductor or dielectric materials, logic and memory devices, neuromorphic devices, quantum devices and quantum enhanced technologies.

3. 2.5D & 3D Stacking, TSV, Backside Power Delivery Network

ESD Issues and solutions in 2.5D & 3D IC packaging and integration, interconnects, TSV, ESD protection requirements in Backside Power Delivery Network.

4. Analog & Automotive Technologies: Bipolar, RF, High Voltage, and BCD

ESD Issues, on-chip ESD protection devices and techniques, IC Design and layout issues, ESD circuit simulation and co-design, DC/Transient Latch-up Issues and Solutions in Bipolar, RF, High Voltage, and BCD Technologies.

5. ESD Testing

ESD Testing trends with Technology Scaling, Multi-dimensional packaging, ESD Test and Characterization method, Traditional and Novel TLP Testing System, HBM and CDM testing issues and solutions, Reliability Test equipment,New failure mechanism, Advance failure analysis techniques, ESD Checking and verification Technology.

6. ESD Device & System Modelling

System level Test, modeling and simulation method, Circuit level design and simulation of ESD Events in Advanced CMOS Technologies, Use of EDA tools, IC Design and Layout issues, Transient ESD induced upset, Robustness evaluation for standard test boards,Large scale analysis with machine and deep learning.

7. Numerical Modeling and Simulation of ESD Components

Component level ESD design including but not limited to SCR, LDMOS, GGNMOS, GDPMOS, Diode, etc., TCAD/Circuit Simulation, Numerical modeling and Physics od ESD events, Advance simulation technologies (SOI, SiGe, FinFET, Compound, Nanowire),Latchup detection prevention and mitigation, Simulation tools and methodology.

8. ESD CAD & Verification

ESD modeling, design guidelines, testing standards, whole chip ESD protection, design verification, compliance testing, ESD Protection for mixed voltage applications.

9. System Level ESD

System efficient ESD design (SEED), ESD testing standards (IEC), co-design methodology of on-board and on-chip ESD protection, ESD protection for consumer electronics, automotive, aerospace and industrial applications, Advancements in System level IEC qualification test methods like Air-discharge tests, Development challenges related to off-chip protection elements with ultra-low capacitances.

10. ESD and EOS Protection in GaN HEMTs & GaN Power ICs

GaN technology based ESD protection diodes, TVS, testing and shielding techniques, EOS protection from overvoltage conditions, current surges and power supply instability.

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Key Dates

May 25th	Poster Submission
May 31st	Poster Acceptance
June 01st	Program Announcement
August 25th	Early Bird Registration Deadline
Sept 05th	Late Registration Deadline
Sept 7th - 8th	India ESD Workshop

InEW 2026 India ESD Workshop

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Pre-Conference Tutorial

Mode: Online
Start Date: August 30th
Eligibility: Available only to those who register for the 7th India ESD Workshop
Speakers: Shreenidhaa K K and Shravya N Raj (Indian Institute of Science)

Tutorial on On-Chip ESD Device & Circuit Design

Designing on-chip ESD protection devices and circuits is a highly specialized field. While this knowledge is accessible through academic research and industry forums, it remains niche and is often shared within limited circles of experts. Many engineers and professionals, even those with some exposure to ESD-related domains, may not have direct experience with ESD device physics or circuit design methodologies. Over the years, participants of the India ESD Workshop (InEW) have consistently expressed that while the workshop offers advanced, in-depth technical content, those without a strong foundation in ESD often find it challenging to follow. Recognizing this gap, we have received repeated requests to offer introductory material that can help participants build the necessary foundational knowledge before attending the workshop. In response to this valuable feedback and with over a thousand participants having benefited from InEW over the years, we are excited to announce that free online tutorial sessions will be offered two weeks prior to the start of the 6th India ESD Workshop (InEW). These tutorials are designed to cover the basics of ESD device physics and circuit design, enabling all registered participants to better engage with and benefit from the advanced content presented during the main event.

Eligibility: All individuals registered for the 7th InEW will receive access to these live online tutorials.

We believe this initiative will significantly enhance the learning experience and help foster a broader and more inclusive ESD design community.

1) Fundamentals of ESD and ESD Design – 4 Hrs

- Introduction to EOS/ESD and Factory measures
- Test standards (HBM, CDM, MM)
- TLP for Device Modeling and Characterization
- ESD Design Window
- ESD Consequences and Simplified ESD Protection Strategy
- ESD Protection with Ground Separation and Multiple Power Rails
- ESD protection for Digital I/Os, Rail Based ESD and Local Clamp Protection, Inter/Intra Domain ESD Stress, b/w Power Rails, Package level Protection Measures, System in Package

2) High Current Device Physics Under ESD Condition – 6 Hrs

- Basic ESD Devices – (1) Resistor, (2) Diode, (3) SCR and (4) ggNMOS
- Advanced ESD Devices – (1) BJT and (2) DeMOS/LDMOS

3) ESD Protection Circuit Design Concepts and Strategy – 4 Hrs

- Qualities of Good ESD Protection
- RCMOS Based Power Clamp Design
- ESD Protection Design Methods – (1) Local Clamps and (2) Rail-to-Rail Clamps
- Diode Based Clamps, ggNMOS Based Clamps, SCR Based Clamps, Fail Safe Protection, HV ESD protection, p-DeMOS Based Clamps
- Secondary Protection Design
- Other Considerations

Click on link to Register: ***https://inew.gtek4u.com/***

www.iisc-inew.org

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Program Schedule

Day 1 (07th September, Monday)

Time	Duration	Speaker & Affiliation	Talk Details
09:15 AM	30 Mins	**Welcome and Inaugural Address**	
09:45 AM	45 Mins	**Dr. Harald Gossner** (Intel, Germany)	ESD Targets and Testing methods for D2D Interfaces (Keynote)
10:30 AM	30 Mins	**Prof. David Pommerenke** (Graz University of Technology)	Measurement of currents and fields of CDM discharges with > 20 GHz bandwidth* (Invited)
11:00 AM	30 Mins	**Break**	**Break**
11:30 AM	30 Mins	**Dr. Sergej Bub** (Nexperia Germany GmbH, Germany)	ESD Protection and ESD Simulation for Automotive Interfaces (Invited)
12:00 PM	30 Mins	**Dr. Dolphin Abessolo Bidzo** (NXP Semiconductors, Netherlands)	ESD Robustness Challenges for RF and High-Speed I/O Applications* (Invited)
12:30 PM	30 Mins	**Prof. Susanna Reggiani** (University of Bologna, Italy)	TCAD-based physical modeling of SCR-LDMOS improving ESD protection with high holding voltages (Invited)
01:00 PM	90 Mins	**Networking Lunch**	**Networking Lunch**
02:30 PM	30 Mins	**Mr. Leonardo Di Biccari** (STMicroelectronics, Italy)	Charge trapping mechanism in thick oxide of HV LDMOS under CDM events* (Invited)
03:00 PM	30 Mins	**Shravya N Raj** (Indian Institute of Science)	Why Schottky Contact in LDMOS Protects It From Filament-Driven Catastrophic ESD Failure? (Ph.D. Talk)
03:20 PM	20 Mins	**Mayank Yadav** (Indian Institute of Science)	Junction Engineered FinFET SCR for Ultimate Tunability of Trigger and Holding Voltage (Ph.D. Talk)
03:40 PM	20 Mins	**Harihar Nath** (Indian Institute of Science)	Physics Based Modeling of Space Charge Modulation Snapback Phenomenon in the TLP Characteristics of HV LDMOS Devices (Ph.D. Talk)
04:00 PM	20 Mins	**Mitesh Goyal** (Indian Institute of Science)	Engineering SCR for better transient characteristics and for high area efficiency (Ph.D. Talk)
04:20 PM	25 Mins	**Coffee Break**	**Coffee Break**
04:45 PM	60 Mins	Panel Moderator: **Dr. Charvaka Duvvury** (It2 Technologies, USA)	Growing ESD Challenges in Next Generation Semiconductor Technologies
05:45 PM	90 Mins	**Poster Session**	
07:15 PM	120 Mins	**Chair's Reception & Dinner**	

* In online mode

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Program Schedule

Day 2 (08th September, Tuesday)

Time	Duration	Speaker & Affiliation	Talk Details
09:00 AM	45 Mins	**Christopher Almeras** (ESD Technologist, Raytheon, United States)	Optimizing the Effectiveness of an ESD Control Program Through Enhanced Training* (Keynote)
09:45 AM	45 Mins	**Dr. Charvaka Duvvury** (iT2 Technologies, USA)	Celebrating 20 Years of Influencing ESD Targets, Standards, and Test Methods (Keynote)
10:30 AM	30 Mins	**Dr. Mirko Scholz** (Infineon Technologies AG, Germany)	System level ESD protection for high-speed data lines (Invited)
11:00 AM	30 Mins	**Break**	**Break**
11:30 AM	30 Mins	**Prof. Isabella Rossetto** (University of Padova, Italy)	Investigation of ESD effects on normally-off p-GaN gate power HEMTs by TLP analysis and numerical simulation (Invited)
12:00 PM	30 Mins	**Dr. Matteo Buffolo** (University of Padova, Italy)	Effects of ESDs on GaN LEDs: a device perspective (Invited)
12:30 PM	30 Mins	**Dr. Milind Furia** (Micron Technology, USA)	Need for reducing ESD targets for Memory Components (Invited)
01:00 PM	90 Mins	**Networking Lunch**	**Networking Lunch**
02:30 PM	30 Mins	**Dr.-Ing. Andreas Hardock** (Nexperia Germany GmbH, Germany)	Optimizing Signal Integrity when Using ESD Protection Devices (Invited)
03:00 PM	30 Mins	**Dr. Sergej Bub** (Nexperia Germany GmbH, Germany)	High-Speed Interface Design – Balancing Signal Integrity and ESD Robustness. Part 2: Optimizing ESD Robustness (Invited)
03:30 PM	30 Mins	**Dr. Joost Willemen** (Infineon Technologies, Germany)	Characterizing TVS Devices for Antenna Protection: ESD Robustness Meets RF Linearity (Invited)
04:00 PM	30 Mins	**Coffee Break**	**Coffee Break**
04:30 PM	10 Mins	**Mr. M M C Kishore** (Global Marketing Services)	Tools for Emerging Technologies in chip fabrication, assembly and characterization (Platform Presentation)
04:40 PM	10 Mins	**Mr. Thomas Tatry** (SENTECH Instruments, Germany)	SENTECH Instruments - Experts in Plasma process and thin Film metrology (Platform Presentation)
04:50 PM	10 Mins	**Mr. Sabarigresan Murugan** (Park Systems India)	Nanoscale Failure analysis using AFM (Platform Presentation)

*** In online mode**

InEW 2026 India ESD Workshop

Program Schedule

Day 2 (08th September, Tuesday)

Time	Duration	Speaker & Affiliation	Talk Details
05:00 PM	15 Mins	**Dr. Vasu Duvvury** (University of North Texas, USA)	Art and Symbolism of the Hand Fan: Its Global and Historical Importance (Contributed Talk)
05:15 PM	15 Mins	**Mr. Harshit Dhakad** (Intel)	From Simulation to Silicon: RF ESD design and characterization for Wifi transceiver (Contributed Talk)
05:30 PM	15 Mins	**Mr. Srinivasamuni Adepu** (ASIC, SanDisk Corporation)	ESD Protection: Layout Challenges, Verification, and Silicon Learnings (Contributed Talk)
05:45 PM	15 Mins	**Mr. Prashanth** (ESD Engineer, Marvell Technology)	3D ESD PERC Verification in Advanced Packaging (Contributed Talk)
06:00 PM	15 Mins	**TBD**	TBD (Contributed Talk)
06:15 PM	15 Mins	**TBD**	TBD (Contributed Talk)
06:30 PM	15 Mins	**Concluding Remarks & Vote of Thanks & 7th InEW Announcement**	
06:45 PM	15 Mins	**Networking, Poster, Hi-tea, and See You @ 8th InEW**	

*** In online mode**

Panel Discussion

Panel Discussion: Growing ESD Challenges in Next Generation Semiconductor Technologies
Date & Time: 7 September, 2026 | 04:45 PM to 05:45 PM
Moderator: **Dr. Charvaka Duvvury** (It2 Technologies, USA)

Session Overview

The semiconductor industry is undergoing rapid advancements, with new technologies pushing the boundaries of what is possible. However, these advancements also bring about new challenges, particularly in the realm of Electrostatic Discharge (ESD) protection. As semiconductor devices become smaller, faster, and more integrated, the need for robust ESD solutions becomes more critical. This panel session will bring together leading experts from academia and industry to discuss and debate the emerging ESD challenges associated with next-generation semiconductor technologies.

Panellists & Topics

Mr. Milind Furia (Micron Technology, USA)
Topic: Discussion on the evolution of CMOS nodes over the next 15 years, focusing on advanced and 3D packaging, heterogeneous integration, backside power rails, and the impact of newer materials like 2D materials on ESD design and protection.

Dr. Sergej Bub (Nexperia GmbH, Germany)
Topic: Exploration of ESD challenges in advanced automotive nodes, system-level ESD issues in electric vehicles (EVs), and the specific requirements of advanced automotive and EV applications.

Dr. Harald Josef Erhard Gossner (Intel Corporation, Germany)
Topic: Examination of the growing complexity of ESD issues and the role of advanced computational and simulation techniques in addressing these challenges. Emphasis on the need for more sophisticated simulation approaches as semiconductor technologies continue to evolve.

Dr. Mirko Scholz (Infineon Technologies AG, Germany)
Topic: Insight into the unique ESD challenges posed by next generation and futuristic technologies. Discussion on the critical role that academia plays in addressing scientifically challenging problems that are beyond the current capabilities of industry, and the importance of industry-academia collaborations.

Session Format

- **Opening Statements (30 minutes):** Each panellist will present their thoughts on the designated topics, providing insights into the current state of ESD challenges and future directions. (7 minutes per panellist with a 30-second buffer for transitions).
- **Panel Debate & Discussion (10 minutes):** Panellists will engage in a debate, discussing and potentially challenging or supporting each other's views on the topics presented.
- **Audience Q&A (20 minutes):** The session will conclude with an interactive Q&A segment, allowing the audience to pose questions to the panellists and participate in the discussion.

Expected Outcomes

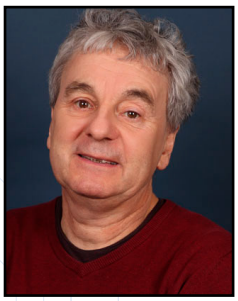
- Provide a comprehensive overview of the current and future ESD challenges in advanced semiconductor technologies.
- Facilitate a deep discussion on the role of emerging technologies in shaping ESD protection strategies.
- Encourage collaboration between industry and academia to address these challenges effectively.

Keynote & Invited Talks

Dr. Harald Josef Erhard Gossner
Intel Corporation, Germany

Talk Title: ESD Targets and Testing methods for D2D Interfaces

Abstract: Complex heterogeneously integrated system in package with hundred thousand to millions of die-to-die interfaces are key for innovative, high-performance Ai CPU and GPU components. Also, across the full spectrum of ICs the usage of chiplets applying die-to-die interfaces will become a driver of innovation. A critical aspect for design is the ESD protection concept where the sheer number of die-to-die interfaces strongly limits the area for protection and the parasitic capacitance. Industry Council on ESD Target levels has proposed a roadmap to 5 V CDM moving to 3V CDM from 2028 on as target level for die-to-die interfaces. An even more fundamental issue is the inability to perform an exhaustive ESD qualification test of these dies due to extremely small pitch of the hybrid bonds of less than 3 µm and the challenge of testing millions of interfaces for one sample. These fundamental questions have recently bene addressed by research and standardization efforts. These are affecting already todays IP and SoC design. The current status and an outlook are provided by the talk.



Prof. David Pommerenke
Graz University of Technology

Talk Title: Measurement of currents and fields of CDM discharges with > 20 GHz bandwidth ✷

Abstract: With heterogenous integration the interest in CDM discharges below 100V is growing. The low voltages and small chiplets lead to rise times below 15ps. To capture these rise times new antennas and current sensors are needed. The talk will present an antenna that operates from 0.4-60+ GHz and a new current target with > 25 GHz bandwidth. The capture devices and captured CDM data will be presented.

Dr. Sergej Bub
Nexperia Germany GmbH

Talk Title: ESD Protection and ESD Simulation for Automotive Interfaces

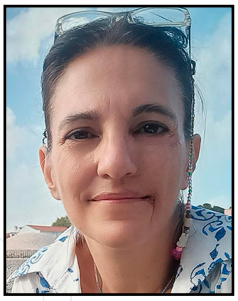
Abstract: This invited talk examines ESD protection for automotive interfaces using System Efficient ESD Design (SEED) simulations and best-practice matching strategies for off- and on-chip solutions to predict and optimize system-level ESD robustness. It introduces the SEED methodology, reviews common automotive protection concepts and tools, and discusses typical failure scenarios and system model setups. Emphasis is placed on behavioural modelling of external ESD devices, including parameter extraction and tuning based on Transmission Line Pulse (TLP) data. Finally, SEED simulations are demonstrated for modern automotive Ethernet and CAN buses, highlighting the impact of component placement, common-mode chokes, and matching challenges between off- and on-chip protection in high-speed systems.

Keynote & Invited Talks

Dr. Dolphin Abessolo Bidzo
NXP Semiconductors, Netherlands

Talk Title: ESD Robustness Challenges for RF and High-Speed I/O Applications ✷

Abstract: The continued aggressive scaling of high-speed and RF I/O bandwidth is critical for the industry. However, achieving higher bandwidth with increasing data rates, while maintaining acceptable power consumption, area efficiency, and reliability, presents significant design challenges. This is due to the very limited ESD protection capacitance load “budget” of those pins for functional reasons. Thus, the ESD protection capability of ultra-high-speed and RF I/Os is impacted. Furthermore, with the gate oxide breakdown voltage trending downwards with each new advanced CMOS technology node, devices are more vulnerable to ESD strikes. This presentation will give an overview of RF ESD design techniques and trade-offs and will show the required transient CDM simulation of RF I/O’s. The CDM level for ultra-High-Speed I/O interfaces will also be discussed.



Prof. Susanna Reggiani
University of Bologna

Talk Title: TCAD-based physical modeling of SCR-LDMOS improving ESD protection with high holding voltages

Abstract: Emerging applications, such as automotive electronics, power management, driver integrated circuits, require ESD protection cells with relatively high trigger and holding voltages in a wide range of operating biases, leading to the need for a family of ESD cells providing optimized performance and minimum occupation area, which is still very challenging. The key element in BCD technology is the LDMOS device with additional integrated SCR. To establish the relevant trade-off between the key parameters, a figure of merit (FOM) is adopted along with dynamical crucial parameters. 2D/3D TCAD simulations are required for a deep physical interpretation of the device behaviour under high injection regimes up to the thermal failure. The proposed physically-based approach will be detailed with some recent examples.

Mr. Leonardo Di Biccari
STMicroelectronics, Italy

Talk Title: Charge trapping mechanism in thick oxide of HV LDMOS under CDM events ✷

Abstract: Oxide charge trapping is deeply investigated phenomenon for IC reliability, considering different scenario than nanosecond time domain. In this work the charge trapping mechanism in HV LDMOS thick oxide under nanosecond event is investigated, by means of characterizations and TCAD simulations. Impact of different CDM test methods and procedures is discussed. This work provides meaningful results for the reliability of the HV ICs, highlighting the impact of the charge trapping phenomenon on HV devices’ physics in case of fast events, and introduces the potential consequences in terms of the IC ESD testing.

Keynote & Invited Talks

Mr. Christopher Almeras
Raytheon, United States

Talk Title: Optimizing the Effectiveness of an ESD Control Program Through Enhanced Training✷

Abstract: ANSI/ESD S20.20 requires an organization's ESD Control Program to establish a Training Plan that includes initial and recurrent training. Despite the importance of this requirement, training is one of the most underutilized tools in the protection of ESD sensitive items. This presentation covers additional training strategies to optimize the effectiveness of an ESD Control Program.

Dr. Charvaka Duvvury
iT2 Technologies

Talk Title: Celebrating 20 Years of Influencing ESD Targets, Standards, and Test Methods

Abstract: Founded in 2006 by just four companies, the Industry Council on ESD Target Levels has made significant strides in advancing the ESD community. This anniversary presentation will summarize the early achievements and the latest developments in the work over the last 5 years. First, we review how the HBM and CDM changes were initiated, and the overwhelming data analysis that overcame the most common resistance to lowering these target levels, which are critical for high-speed performance circuits. The talk will then move on to other topics in EOS and System Level misunderstandings, and the critical achievements that establish clear insight into these areas. The most important part of the seminar will describe the complex topic of "transient Absolute Maximum Rating" (tAMR) and the controversy surrounding it, which has led to a clearer understanding after nearly 5 years of debate. For both EOS safety and IC customer applications, a tAMR that allows pulses exceeding the common AMR is critical. Another recent important topic has been "Direct Pin System Level ESD Testing". These two topics are the crowning achievements of the Council since 2020 and require thorough industry appreciation to improve the reliability of electronic systems into the next decade.

Dr. Mirko Scholz
Infineon Technologies AG, Germany

Talk Title: The ESDA Technology Roadmap

Abstract: The ESDA technology roadmap aims to support and guide the daily work of ESD and latchup experts in the worldwide industry and academia. It discusses ESD target level and their impact on ESD control practices. Next to regular updates on ESD testing standards the focus of the document is on technical challenges in our industry. In this talk we will provide an update on the 2027 edition and give an outlook on the ESD and Latchup challenges for the coming years.

Keynote & Invited Talks

Prof. Isabella Rossetto

University of Padova, Department of Information Engineering, Italy

Talk Title: Investigation of ESD effects on normally-off p-GaN gate power HEMTs by TLP analysis and numerical simulation

Abstract: In this work we will present the effect of electrostatic discharge (ESD) on GaN power HEMTs with Schottky gate metal. The device robustness and the impact of the device geometry is discussed. The root causes of the degradation processes are investigated by transmission line pulse (TLP) system, numerical simulation and deep level characterization techniques.

Dr. Matteo Buffolo

University of Padova - Department of Information Engineering, Italy

Talk Title: Effects of ESDs on GaN LEDs: a device perspective

Abstract: Over the last 25 years, the reliability of LEDs based on nitride semiconductors has vastly improved, allowing state of the art devices emitting in the visible range to reach useful lifetimes in excess of tens of thousands of hours. Hence, for these technologies, extrinsic overstress events, such as ESDs, represent the major cause of failure on the field. While previous studies have somehow investigated the relation between overstress and sudden failures, a lack of literature on the potential latent damage provoked by the non-destructive overstress events is missing. This talk primarily aims to investigate this topic from a physical standpoint, by also leveraging some recent results obtained on visible InGaN/GaN LEDs.

Keynote & Invited Talks

Mr. Milind Furia
Micron Technology, USA

Talk Title: Need for reducing ESD targets for Memory Components

Abstract: Memory interfaces are approaching per-pin data rates where the ESD protection network itself becomes a limiting circuit element. On a modern DRAM I/O, the ESD clamp and the interconnect required to reach it are among the largest contributors to pad capacitance, second only to the output driver – and pad capacitance directly governs whether a multi-gigabit link can close its eye. As DDR6 targets the 9.6–19.2 Gb/s range, holding legacy component ESD targets forces a protection network that the channel can no longer afford, while offering no measurable reliability benefit in an EPA (ESD Protected Area) controlled factory. This talk makes the case that component-level HBM and CDM targets for next generation high-speed memory must follow the direction the ESD Association's Technology Roadmap and the Industry Council on ESD Target Levels have documented for a decade. We will review how the ESD risk has moved: a populated DIMM stores far more charge than a single package, so the dominant handling exposure is now a board-level event. Ground-first-contact edge-connector design, module-level charged-board-event testing, and low-voltage contact-CDM methods are presented as the mitigations that let component targets come down safely.

Dr. - Ing. Andreas Hardock
Nexperia Germany GmbH

Talk Title: Optimizing Signal Integrity when Using ESD Protection Devices

Abstract: This part focuses on practical methodologies to preserve signal integrity (SI) while implementing effective ESD protection in high-speed automotive and mobile interfaces. It emphasizes the trade-offs between SI performance and ESD robustness in bandwidth-limited and impedance-controlled systems. A simulation-driven approach is applied using SPICE, IBIS/AMI, and 3D EM tools to evaluate key metrics such as insertion loss, return loss, impedance discontinuities, and eye diagram degradation, with strong correlation to measurement results. Topics include selection and modeling of low-capacitance ESD devices, parasitic effects, and co-design of terminations and filtering networks. PCB layout best practices address parasitics and return paths. Case studies from Ethernet and SerDes illustrate optimization of ESD protection and passive networks while maintaining SI performance.

Keynote & Invited Talks

Dr. Sergej Bub
Nexperia Germany GmbH

Talk Title: High-Speed Interface Design – Balancing Signal Integrity and ESD Robustness. Part 2: Optimizing ESD Robustness.

Abstract: This part addresses system-level ESD challenges in high-speed automotive, mobile, and computing applications, driven by increasing data rates and stringent EMC requirements. Due to scaling and cost limitations, on-chip ESD protection is often insufficient, making external protection essential. The session introduces the SEED (System Efficient ESD Design) methodology, which employs dynamic models and transient simulations to analyse complete systems under ESD stress. It covers system-level modelling approaches, industry-standard simulation tools, and both behavioural and physics-based modelling techniques, including parameter extraction and tuning. The methodology enables accurate prediction and optimization of system-level ESD robustness for high-speed interfaces.

Dr. Joost Willemen
Infineon Technologies, Germany

Talk Title: Characterizing TVS Devices for Antenna Protection: ESD Robustness Meets RF Linearity

Abstract: The increasing integration density of modern RF systems is driving growing demand for dedicated ESD protection at antenna ports of mobile devices. TVS devices represent a promising protection solution, but their suitability for antenna applications extends beyond ESD robustness and clamping performance alone. RF linearity is a critical requirement, as nonlinear device behavior generates unwanted harmonics and intermodulation products that can degrade system performance. This talk examines TVS devices for antenna ESD protection with emphasis on characterization methods and measured device behavior. Key approaches for assessing linearity and harmonic generation are presented, and the underlying mechanisms driving nonlinear behavior are discussed. The results provide insight into the relevant device parameters that determine TVS suitability for RF antenna protection applications.

Platform Presentations

M. M. C. Kishore
Founder and CEO
Global Marketing Services (GMS)

Talk Title: Tools for Emerging Technologies in chip fabrication, assembly and characterisation.

Abstract: Emerging technologies in chip fabrication, assembly, and characterization are driving a new era of semiconductor innovation, enabling higher performance, energy efficiency, and scalability. The rapid evolution of nanoscale devices, heterogeneous integration, and advanced packaging demands novel tools that can address the challenges of precision, throughput, and reliability. In fabrication, processes such as lithography, wet process and other process are critical . Assembly processes are being transformed by 3D integration, wafer-level packaging, and micro-bump bonding, which require ultra-accurate alignment, defect-free interconnects and temporary bonding and debonding . Characterization tools, including wafer warp, x-ray, C-SAM are essential for structural properties for driving quality and reliability. Together, these tools form a synergistic ecosystem that supports the design and deployment of advanced chips for applications in artificial intelligence, quantum computing, and high-performance communication systems. This talk explores the state-of-the-art tools across these domains, highlighting their role in overcoming scaling bottlenecks and enabling the future of semiconductor technology.

Thomas Tatry
Application Engineer
SENTECH Instruments, Germany

Talk Title: SENTECH Instruments - Experts in Plasma process and thin Film metrology

Abstract:SENTECH has over thirty years of experience developing and manufacturing plasma process technology systems and thin film metrology tools for research and development and industrial production worldwide. Our robust systems focus on the etching, deposition, and characterisation of thin films in semiconductor technology, microsystems technology, photovoltaics, nanotechnology, and materials research. The SENTECH flexible and reliable plasma etch and deposition systems, including atomic layer deposition equipment, support state-of-the-art processes and applications. Our tools and systems are used worldwide for applications in the fields of nanotechnology, micro-optics, sensor technology, photonics, and optoelectronics. SENTECH offers a wide range of spectroscopic ellipsometers, laser ellipsometers, and reflectometers for measuring the thickness and optical constants of very thin layers or layer stacks. SENTECH has achieved particular success in the field of industrial quality control, for example in photovoltaics, 5G devices, and sensor technology. For more information or to contact a member of the team, please visit our website www.sentech.de

Platform Presentations

Sabarigresan Murugan
Application Scientist
Park Systems India

Talk Title: Nanoscale Failure analysis using AFM

Abstract: Industry standards now demand near-zero manufacturing downtime, making root-cause analysis for any production defect critical. Advanced Atomic Force Microscopy (AFM) addresses this by enabling nanoscale failure analysis, dopant profiling, and rigorous quality control. This study explores key electrical AFM modes - including Scanning Capacitance Microscopy (SCM), Scanning Spreading Resistance Microscopy (SSRM), and PinPoint Electrical AFM (iAFM) - for high-resolution, precise carrier characterization. Furthermore, we demonstrate that high-vacuum environments, such as the Park NX-Hivac system, significantly reduce contact force, eliminate sample oxidation, extend tip lifetime, and enhance signal-to-noise ratios compared to ambient operations. Additionally, operational enhancements like QuickStep scanning and specialized sample-tilting wedges successfully optimize measurement throughput, minimize thermal drift, and enable accurate characterization of complex device topographies, including FinFETs and vertical sidewall structures.

Dr. Vasu Duvvury
Professor (Retired)
University of North Texas, USA

Talk Title: Art and Symbolism of the Hand Fan: Its Global and Historical Importance

Abstract: At the mention of a 'hand fan', one immediately thinks of a mundane and ordinary object that one uses to cool oneself on a warm and summery day. But the utilitarian and decorative fan in many styles has been used by different cultures across civilizations as an aesthetic and cultural object since very ancient times to signify a variety of things in social and religious contexts like status, artistry, social and cultural identity. This talk will explore this fascinating topic with illustrations and pictures of fans both globally and historically.

Harshit Dhakad
Intel

Talk Title: From Simulation to Silicon : RF ESD design and characterization for Wifi transceiver

Abstract: Every Wi-Fi transceiver chip that ships in a laptop or smartphone, carries a hidden design battle - one fought between two competing demands. On one side, the RF circuits need clean, low-loss signal paths to deliver the sensitivity and linearity that modern Wi-Fi standards require. On the other, every chip must survive real-world electrostatic discharge events that can instantly destroy unprotected devices. As CMOS technology scales to smaller nodes, this problem only gets harder to resolve - the design window between adequate ESD robustness and acceptable RF performance keeps shrinking. This talk walks through the complete journey from design intent to ESD qualified silicon and focusses a practical, experience-driven perspective on building ESD protection that a Wi-Fi transceiver can actually live with — robust enough to pass qualification, transparent enough not to compromise the RF performance that the product was designed to deliver.

Srinivasamuni Adepu
Senior IO Layout Manager
Mixed Signal IP group, ASIC, SanDisk

Talk Title: ESD protection:Layout Challenges, Verification and Silicon learnings

Abstract: Electrostatic Discharge (ESD) protection continues to be a critical reliability requirement for advanced-node SoC and IO designs. As IO pad-rings become denser and designs include multiple voltage and power domains, ESD implementation must address layout, routing, verification, and silicon robustness together. This talk will discuss practical layout challenges in IO and pad-ring design, including ESD current path optimization, clamp placement, routing considerations, multi-voltage and multi-power domain handling, and metal/via reliability. It will also cover ESD verification and sign-off methodologies used to identify protection gaps and improve closure confidence. The session will share silicon failures and lessons learned, along with best practices adopted in production designs. The goal is to provide practical guidance for improving ESD robustness, reducing debug cycles, and increasing first-pass silicon confidence.

Prashant Gajbhiye
Staff Engineer - ESD Engineer
Marvell Technology

Talk Title: 3D PERC Verification in Advanced Packaging

Abstract: The increasing adoption of advanced semiconductor technologies and heterogeneous integration has led to the widespread use of multi-die packaging architectures. Ensuring ESD reliability and correct connectivity across such complex systems is a critical challenge. 3D Physical Electrical Rule Checking (3D PERC) provides a comprehensive framework for verifying electrical behavior, connectivity, and reliability across stacked designs consisting of multiple dies, interposers, and substrates. In this work, a methodology for 3D PERC-based system-level verification is presented, focusing on key aspects such as point-to-point (P2P) connectivity checks, topology validation, and resistance-based path verification. The approach enables accurate validation of signal paths and ensures correct electrical behavior across multiple layers of integration. Additionally, ESD-related verification, including discharge path validation and protection network analysis, is incorporated to ensure robust design reliability. The study also highlights challenges associated with 3D PERC verification, including complex multi-layer connectivity, large-scale power/ground networks, and debugging of topology violations. Techniques such as 3D-aware rule configuration, optimized rule implementation, and efficient debug methodologies are applied to improve verification accuracy and runtime efficiency. The proposed approach enables early detection of connectivity and reliability issues and provides a scalable and reusable verification solution for advanced multi-die and packaging technologies. This contributes to improved design robustness and reduced turnaround time in modern semiconductor design flows.

Ph.D. Research Talks

Shravya N Raj
Indian Institute of Science

Talk Title: Why Schottky Contact in LDMOS Protects It From Filament-Driven Catastrophic ESD Failure?

Abstract: In this work, well-calibrated electrothermal 3D TCAD simulations are used to investigate the behavior of Schottky drain LDMOS devices under ESD stress. The study examines ESD robustness for different Schottky drain metal work functions, with particular emphasis on current filament formation and evolution. The impact of drain-side Schottky barrier engineering is analyzed in detail to identify the appropriate metal silicide for achieving enhanced ESD protection. Transient ESD simulations reveal how variations in barrier height influence carrier injection, current spreading, and localized self-heating, which collectively govern filament stability and failure onset. The results provide physical insight into filament-driven catastrophic failure mechanisms and demonstrate that optimized Schottky drain design can effectively suppress current localization and improve ESD robustness.

Mayank Yadav
Indian Institute of Science

Talk Title: Junction Engineered FinFET SCR for Ultimate Tunability of Trigger and Holding Voltage

Abstract: Junction-Engineering for fin-based silicon controlled rectifier (FinSCR) architectures for on-chip ESD protection is proposed in this work to achieve a wide range of holding and trigger voltages without compromising the failure current. In this novel proposal, low dose higher energy deep implants are placed underneath fins. P+ is replaced with an N+ at the Anode/NTAP and N+ with P+ at the Cathode/PTAP of FinSCR to form additional p-n or n-p junctions beneath fins in the n-well and p-well region. These junctions provide the junction potential in the well region to manipulate the bipolar efficiency of parasitic PNP and NPN. Detailed physical insight is explained on holding and trigger voltage tunability for junction-engineere architecture. Besides, the proposed concept, together with the number of fins of the Anode/Cathode or NTAP/PTAP, offers the ultimate tunability.

Ph.D. Research Talks

Harihar Nath
Indian Institute of Science

Talk Title: Physics Based Modeling of Space Charge Modulation Snapback Phenomenon in the TLP Characteristics of HV LDMOS Devices

Abstract: A physics-based analytical model is developed for capturing the phenomenon of space charge modulation in the intrinsic NPN of the LDMOS device for a 100 ns TLP stress. Reverse-biased base–collector avalanche, current partitioning through the emitter diode and base resistance, and space charge modulation by injected electrons are coupled self-consistently to reproduce the snapback phenomenon and to form the basis for current filament formation. Model Validation was also done by varying the n-well region's doping.

Mitesh Goyal
Indian Institute of Science

Talk Title: Engineering SCR for better transient characteristics and for high area efficiency

Abstract: In this talk, various engineering methods to improve the ESD characteristics of SCR are discused. Firstly, a novel gate and substrate triggered silicon-controlled rectifier (SCR) with improved transient characteristics for electrostatic discharge (ESD) protection concepts is presented and secondly, an area efficient implementation of the SCR with tunable trigger voltage is presented. The ESD local protection concepts are presented with co-engineered devices and trigger circuits resulting in lower peak voltages, improved turn-on times and higher area efficiency when compared to known reference ESD protection concepts. Previous works related to SCR have concentrated on quasi static TLP/vf-TLP parts and very little work is published to improve the transient characteristics of the ESD characteristics. The proposed and reference concepts are implemented in Samsung 28 nm process for experimental validation and benchmarking. TLP/vf-TLP and other ESD/DC measurement results along with the design guidelines and trade-offs are presented in this paper. The proposed concept can realize the demanding I/O needs of SCR based local clamps, qualified for HBM to CDM time domains, and meeting ESD specs required for high speed I/Os buffers.

Poster Presentations

Design and Implementation of Bidirectional Ultra Low Capacitance Transient Voltage Suppressor Diode for System Level ESD Protection

G Yashan Kumar, Rathin Mahesh Ghivari, Ajinkya Sadavarte, Sandip Lashkare
(IIT Gandhinagar)

Abstract: Electrostatic Discharge (ESD) protection safeguards microelectronic devices from fast, high-voltage/current transients that can cause catastrophic failure in integrated circuits. For high-frequency applications, ESD protection devices should withstand high ESD levels while maintaining ultra-low capacitance (ULC) to maintain signal integrity. Conventional ESD protection devices use Zener and PN diodes. These devices provide good protection but exhibit high capacitance (1–6 pF), which slows down the device response. Further, many applications would require bidirectional ESD protection, which adds additional limitations. In this work, a bidirectional ULC TVS diode is studied and analyzed for ESD failure levels, along with its capacitance performance, for high-speed applications. The ESD handling capacity is analyzed using Transmission Line Pulse (TLP) measurements, which provide an in-depth understanding of the TVS diode's physical behavior and failure mechanisms. A PCIe test case is used as a reference for demonstration with a fixed breakdown voltage. The ESD device has an area of 450 × 1 μm², is capable of handling an ESD current of 0.27 A/μm, and exhibits a total parasitic capacitance of 3.87 mF/μm. These ultra-low capacitance TVS diodes offer robust ESD protection and signal integrity, making them suitable for high-frequency applications. However, the same methodology can be applied to other high-speed applications such as USB, HDMI, Thunderbolt, CAN, and LIN, which operate at different voltages.

Mitigation of Gate Oxide Overstress during CDM Events using a Novel ESD Protection Structure in High-Speed RX Drivers

Saloni Rana
(Marvell India Private Limited, Bangalore)

Abstract: Gate oxide reliability during Charged Device Model (CDM) events remains a critical challenge in deeply scaled high-speed interface circuits. Detailed ESD simulations identified excessive transient stress at an internal high-impedance decoder-driven PFET gate node caused by transient charge buildup and inadequate discharge paths during CDM events. To address this, a novel ESD mitigation structure was introduced to provide an effective transient clamp path without impacting normal operation. Simulation results demonstrate reduced peak gate stress, improving gate oxide reliability and overall ESD robustness in advanced high-speed RX drivers.

TCAD Study of a floating-p SCR-LDMOS Device

Giacomo Drudi
(University of Bologna)

Abstract: A new SCR-LDMOS device is investigated through 2D and 3D TCAD simulations to obtain maximum holding voltage, minimum area and high ESD robustness. The effect of the additional floating-p region is studied analyzing the carrier and electric field distribution in the device with simulations. Reduced overvoltage and improved turn-on time are observed in the very-fast pulsed regime with respect to the device without floating-p. Tunability of holding voltage with drift length is shown. 3D effects are studied showing improved ruggedness to premature failure during snapback by mitigating current filamentation.

Improving Robustness of Dynamic ESD Clamps Against False Activation

Sanket Sonar
(STMicroelectronics)

Abstract: Dynamic ESD clamps are essential for protecting integrated circuits, but their ramp rate sensitive behavior can lead to false triggering during normal operation of Fail-safe and non Fail-safe IOs. This work investigates robustness issues in both non-floating-rail and floating-rail clamp architectures, especially under fast functional supply ramps, glitches, and biased-rail disturbances. Different design approaches are presented to suppress unintended activation: a disable circuit referenced to an always-on or earlier-rising supply and a dual-condition trigger combining ramp-rate and voltage detection or use of diode to avoid false triggering. These techniques improve immunity to false turn-on while preserving ESD protection effectiveness. Trade-offs in area, tuning complexity and clamping voltage are discussed to guide application specific implementation choices.

Design & Implementation of Programmable Transmission Line Pulse Generation Technique

Amitabh Chatterjee
(Shiv Nadar University)

Abstract: In our work we present designing a Transmission Line Pulser (TLP) that employs ultra-fast switching components to produce high-voltage, rectangular pulses. It delves into the fundamental physics of DC charging and discharging into a load, while providing practical mathematical formulas for calculating pulse width and amplitude. Design & Implemnetation explores various semiconductor options, such as avalanche transistors and GaN FETs, and emphasizes specific layout strategies with ability to control the pulse rise-time meeting HBM & CDM ESD standards. In addition to hardware implementation, the source details modeling for simulating electronic behavior and includes a thorough section on high-voltage safety protocols. Ultimately, these guidelines offer a comprehensive framework for engineering precision pulse generators used in ESD device testing and characterization.

Why Schottky Contact in LDMOS Protects It From Filament Driven Catastrophic ESD Failure?

Shravya N Raj
(Indian Institute of Science)

Abstract: In this work, well-calibrated electrothermal 3D TCAD simulations are used to investigate the behavior of Schottky drain LDMOS devices under ESD stress. The study examines ESD robustness for different Schottky drain metal work functions, with particular emphasis on current filament formation and evolution. The impact of drain-side Schottky barrier engineering is analyzed in detail to identify the appropriate metal silicide for achieving enhanced ESD protection. Transient ESD simulations reveal how variations in barrier height influence carrier injection, current spreading, and localized self-heating, which collectively govern filament stability and failure onset. The results provide physical insight into filament-driven catastrophic failure mechanisms and demonstrate that optimized Schottky drain design can effectively suppress current localization and improve ESD robustness.

3D PERC Verification in Advanced Packaging

Prashant
(Marvell Semiconductor India)

Abstract: The increasing adoption of advanced semiconductor technologies and heterogeneous integration has led to the widespread use of multi-die packaging architectures. Ensuring ESD reliability and correct connectivity across such complex systems is a critical challenge. 3D Physical Electrical Rule Checking (3D PERC) provides a comprehensive framework for verifying electrical behavior, connectivity, and reliability across stacked designs consisting of multiple dies, interposers, and substrates. In this work, a methodology for 3D PERC-based system-level verification is presented, focusing on key aspects such as point-to-point (P2P) connectivity checks, topology validation, and resistance-based path verification. The approach enables accurate validation of signal paths and ensures correct electrical behavior across multiple layers of integration. Additionally, ESD-related verification, including discharge path validation and protection network analysis, is incorporated to ensure robust design reliability. The study also highlights challenges associated with 3D PERC verification, including complex multi-layer connectivity, large-scale power/ground networks, and debugging of topology violations. Techniques such as 3D-aware rule configuration, optimized rule implementation, and efficient debug methodologies are applied to improve verification accuracy and runtime efficiency. The proposed approach enables early detection of connectivity and reliability issues and provides a scalable and reusable verification solution for advanced multi-die and packaging technologies. This contributes to improved design robustness and reduced turnaround time in modern semiconductor design flows.

Area Efficient Substrate Triggered SCR Based Local ESD Clamp Concepts with Tunable Trigger Voltage

Mitesh Goyal
(Indian Institute of Science)

Abstract: An area-efficient substrate-triggered silicon-controlled rectifier (EPDSCR) device is presented for electrostatic discharge (ESD) protection in high-speed I/O applications. The device employs a co-engineered SCR structure and trigger circuit for enabling IO-VSS and IO-VDD local clamps, with reduced and tunable trigger voltage while maintaining low parasitic capacitance. By optimizing the substrate triggering mechanism and SCR conduction path, the proposed design achieves higher ESD robustness per unit area, lower on-resistance, and improved current handling capability compared to state-of-the-art SCR-based protection schemes. The reduced parasitic capacitance makes the device suitable for high-speed interfaces. The proposed concept is implemented and validated using multiple test chips fabricated in a 28-nm bulk CMOS process. Measurement results from TLP, vf-TLP, and DC characterization confirm enhanced IT2, reduced VT1, and improved ESD performance. The proposed EPDSCR meets the ESD requirements of modern I/O interfaces and provides robust protection across HBM and CDM stress conditions.

Physics Based Modeling of Space Charge Modulation Snapback in HV LDMOS Devices

Harihar Nath
(Indian Institute of Science)

Abstract: A physics-based analytical model is developed for capturing the phenomenon of space charge modulation in the intrinsic NPN of the LDMOS device for a 100 ns TLP stress. Reverse-biased base–collector avalanche, current partitioning through the emitter diode and base resistance, and space charge modulation by injected electrons are coupled self-consistently to reproduce the snapback phenomenon and to form the basis for current filament formation. Model validation was also done by varying the n-well region's doping.

Unification of Filament Dynamics in LDMOS Devices across Voltage Classes

Shreenidhaa K K
(Indian Institute of Science)

Abstract: Laterally-Diffused MOS (LDMOS) transistors are highly susceptible to electrostatic discharge (ESD) stress, with device failure primarily attributed to catastrophic filament formation leading to thermal runaway. Previous studies have examined the underlying filament formation and failure mechanisms independently for different voltage classes. Though the underlying physics is the same, there are ambiguities related to the slight differences in the filament dynamics with respect to different voltage classes. In this work, a unified framework is proposed to correlate and generalize the filament behaviour of LDMOS devices across multiple voltage classes. The analysis is carried out on devices with systematic doping variations within the drift region, enabling a comprehensive understanding of the failure dynamics as a function of voltage class.

Junction Engineered FinFET SCR for Ultimate Tunability of Trigger and Holding Voltage

Mayank Yadav
(Indian Institute of Science)

Abstract: Proposed a junction-engineered FinSCR architecture for on-chip ESD protection with tunable holding and trigger voltages. Introduced deep implants and additional p–n/n–p junctions beneath fins to control parasitic PNP/NPN transistor behaviour. Achieved flexible ESD performance optimisation while maintaining high failure current capability through junction engineering and fin-count adjustment.

Ultra-fast TLP characterization of gate-all[1]around (GAA) ESD diodes for low-capacitance optimized I/Os

Anish K Kumar, Krzysztof Domanski, Raj S Dua, Reshma R Menon, Umair Ishfaq, Salukazi Shamutete, Florian Klotz, Harshit Dhakad and Anand Sharma
(Intel)

Abstract: This paper presents the characterization and modeling of diodes fabricated using bulk and gate-all-around (GAA) technologies, highlighting the enhanced electrostatic discharge (ESD) robustness observed in the GAA FINFET node. Ultra-fast Transmission Line Pulse (uf-TLP) measurements with rise times of 40ps, and very-fast TLP (vf-TLP) measurements with rise times of 100ps were conducted, targeting both diode structures and gate oxide (GOX) victims. Diodes using non[1]planar FINs with bulk node exhibited slower response and higher forward recovery (FR) overshoot, whereas GAA diodes demonstrated faster switching behavior without FR overshoot. GOX structures in the bulk node failed prematurely due to FR-induced stress, in contrast to the more robust performance observed with GAA diodes. The overshoot-free switching of ESD diodes processed in GAA-FINFET Intel technology allows for improvement of several key performance indicators (KPI) in the High Speed (HS) interfaces, as shown on the example of DDR

Ghost Failures or Real Threats? Unmasking the Role of Inadvertent Device Charging in CDM Testing

Harshit Dhakad, Pavel Zisman, Chandrasekhar Korada, Anand Sharma
(Intel)

Abstract: CDM (Charged Device Model) testing is the industry-standard method for qualifying integrated circuits against electrostatic discharge events that occur during automated handling and assembly. However, a less-discussed but practically significant problem exists — devices that arrive at the test setup carrying a residual electrostatic charge from prior handling, storage, or measurement steps or triboelectric charging of DUT within CDM tester. This inadvertent pre-test charging superimposes an additional current/voltage stress on top of the intended CDM pulse, pushing sensitive pins beyond their actual failure threshold and generating failures that would not occur under clean test conditions. This poster investigates the mechanism by which pre-existing device charge contributes to false failures, with particular focus on high-performance pins such as RF inputs, high-speed I/O, and analog signal ports — pins that are inherently more vulnerable due to thin gate oxides, tight ESD design windows, and low parasitic capacitance. Through a combination of controlled experiments, and correlation with failure signatures, we demonstrate that a meaningful fraction of observed CDM failures on these pins can be attributed to pre-test charging artifacts rather than genuine ESD weakness. The findings have direct implications for how CDM test results are interpreted, how test environments should be controlled, and how ESD design margins are set for sensitive pins. Practical recommendation for eliminating pre-test charging effects is discussed, with the goal of improving the reliability and repeatability of CDM qualification in production and characterization environments.

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